AD-A045 819 RCA LABS PRINCETON N J F/G 9/5
A LOGIC MODULE USING TRANSFERRED-ELECTRON LOGIC DEVICES FOR PRE--ETC(U)
SEP 77 W R CURTICE N00039-75-C-0225
UNCLASSIFIED PRRL-77-CR-31 NL

| OF |
ADA045819

END
DATE FILMED
11-77
DDC

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

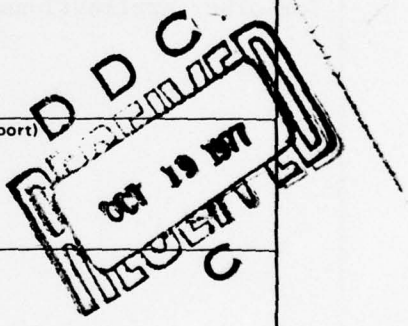
REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) (6) A LOGIC MODULE USING TRANSFERRED-ELECTRON LOGIC DEVICES FOR PRECISION TIME INTERVAL MEASUREMENTS.		5. TYPE OF REPORT & PERIOD COVERED Final Report (2-26-75 to 6-30-77)
		6. PERFORMING ORG. REPORT NUMBER (14) PRRL-77-CR-31 ✓
7. AUTHOR(s) (10) W. R. Curtice		8. CONTRACT OR GRANT NUMBER(s) (15) N00039-75-C-0225 New
9. PERFORMING ORGANIZATION NAME AND ADDRESS RCA Laboratories Princeton, New Jersey 08540		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS (11) Naval Electronic Systems Command Electronics and Special Warfare Div. ELEX 350 Washington, DC 20360		12. REPORT DATE September 1977
		13. NUMBER OF PAGES 72
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) (9) Final rept. 26 Feb 75 - 30 Jun 77		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

(12) 73p.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)



18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Transferred Electron Logic Device (TELD)
MESFET
Time interval measurement
Threshold gate
Coincidence circuit

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The results of a program to develop a logic module using transferred electron logic devices (TELDs) for use in a short baseline time-difference-of-arrival (TDOA) direction finding system are described. The function of the logic module is to perform high precision, single-event time interval measurements. The ultimate goal for precision is 20 ps. The purpose of the present program is to prove feasibility of time

DD FORM 1 JAN 73 1473

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

299 000

LB

measurement with subnanosecond resolution in a breadboard TELD module.

The module's design is based upon the technique of vernier time measurement using two digital processing channels. The arrival of an rf signal above a threshold value at the early channel initiates a pulse burst to be sent to the coincidence circuit. This pulse burst has constant amplitude pulses of fixed width and period T_c. A second pulse train is generated by the vernier channel; however, the period for this group is T_v. If M clock pulses occur before the start of the vernier channel and N clock pulses have occurred at coincidence, then the total time difference, T, is $(M-1)T_c + (N-M)\cdot(T_c-T_v)$.

The two input threshold gates and the coincidence circuit utilize TELDs and the pulse burst generators are constructed with GaAs MESFETs. Step recovery diodes have been used for pulse shaping at several points in the circuit. The counters are commercially available and of ECL type. A thorough study was made of the circuit design of the module's components and the results are contained herein.

A breadboard system was designed, constructed, and tested without the ECL counters. Four pulses were used for each pulse burst generator and $T_c \approx 1.2$ ns. This produced a resolution of about 400 ps which was confirmed in the tests. In these tests the output of the coincidence circuit was observed as the time delay of the rf signal (0.8 GHz) to one channel was varied. The range of measurement (with counters) is about 2 ns, which is adequate for the present application.

It is shown that 100-ps resolution should be obtainable in future designs. The range of time measurements can also be increased significantly for other applications. Critical problem areas are described.

PREFACE

This report describes research done in the Microwave Technology Center of RCA Laboratories, Princeton, New Jersey under Contract Number N00039-75-C-0225 during the period February 26, 1975 to June 30, 1977. F. Sterzer is the Center's Director, S. Y. Narayan was the Project Supervisor and W. R. Curtice was the Project Engineer. The transferred-electron devices utilized in this program have been designed and developed by L. C. Upadhyayula, and fabricated by R. Smith. The experimental circuits were constructed by J. F. Wilhelm, J. E. Brown, P. R. Pelka, O. M. Gervasoni, and N. S. Klein. The MESFET devices were screened and made available by J. J. Napoleon.

Mr. Joseph Kain (ELEX3503) was the program monitor for the Naval Electronic Systems Command, and Mr. H. Crecraft (Code 5725) of the Naval Research Laboratory served as his technical consultant.

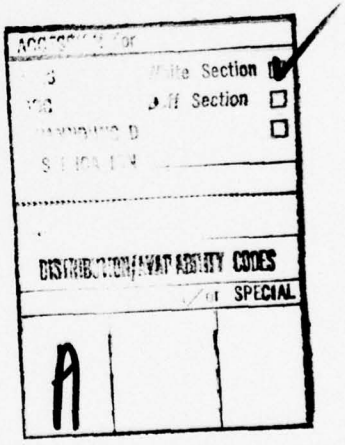


TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

SECTION I

INTRODUCTION

The objective of this program is to develop an ultrahigh-speed logic module which can be used to measure the time-difference-of-arrival (TDOA) of an rf signal at different parts of an antenna array. The logic module employs a vernier time measurement scheme and utilizes the ultrafast switching properties of transferred-electron logic devices (TELDs). The ultimate goal of this program is to produce a time resolution of 20 ps. The present goal is to demonstrate the feasibility of single-event time-difference-of-arrival measurements with subnanosecond resolution for GHz signals.

This report describes the progress made during Phase I, the study phase, and Phase II, the hardware development phase. After a description of the TDOA system and vernier measurement scheme in Section II, Section III describes the experimental evaluation of the breadboard logic module. The design and experimental performance of the subsystems which constitute the logic module are described in Section IV, and the conclusions and recommendations for further work are presented in Section V.

SECTION II

THE TDOA SYSTEM

A. SYSTEM DESCRIPTION

Figure 1 shows a simplified block diagram of a TDOA system. The function of the system is to accurately measure the time-difference-of-arrival (TDOA) of an rf burst at two isotropic antennas. The major parts of the system are: (1) the rf module which consists of matched amplifiers and limiters to increase the signal from the antennas to a level capable of triggering three-terminal TELDs (about 0 to 10 dBM), and (2) the TELD logic module with threshold gates and a vernier counter capable of subnanosecond resolution. The logic module is frequency independent and can be used with rf modules covering different frequency ranges.

Figure 2 shows the major parts of the logic module subsystem. There are two TELD threshold gates which generate start and stop pulses, a vernier and coarse time measurement subsystem, and the digital counter. The TDOA system's resolution, accuracy, and range are determined by the design of these components, which will be discussed later in this report. An ultimate goal of 20-ps resolution is desired. However, feasibility of the concept can be demonstrated with subnanosecond resolution and limited range.

B. THE VERNIER TIME MEASUREMENT SUBSYSTEM

The most critical part of the TDOA system shown in Fig. 1 is the TELD logic module. This consists of matched TELD threshold circuits and a vernier time measurement subsystem. The principles of vernier time measurement systems are well known. D. Martin [1] has presented an excellent discussion of the principles of time interval measurements by various techniques. In addition, R. G. Baron [2] has described a vernier time-measurement technique by which it is possible to measure nonperiodic and asynchronous time intervals accurately.

---

1. D. Martin, "Measure Time Interval Precisely," Electronic Design, 24, 162-167, (November, 1974).
2. R. G. Baron, "The Vernier Time Measuring Technique," Proc. IRE, 45, 21-30, (January, 1957).

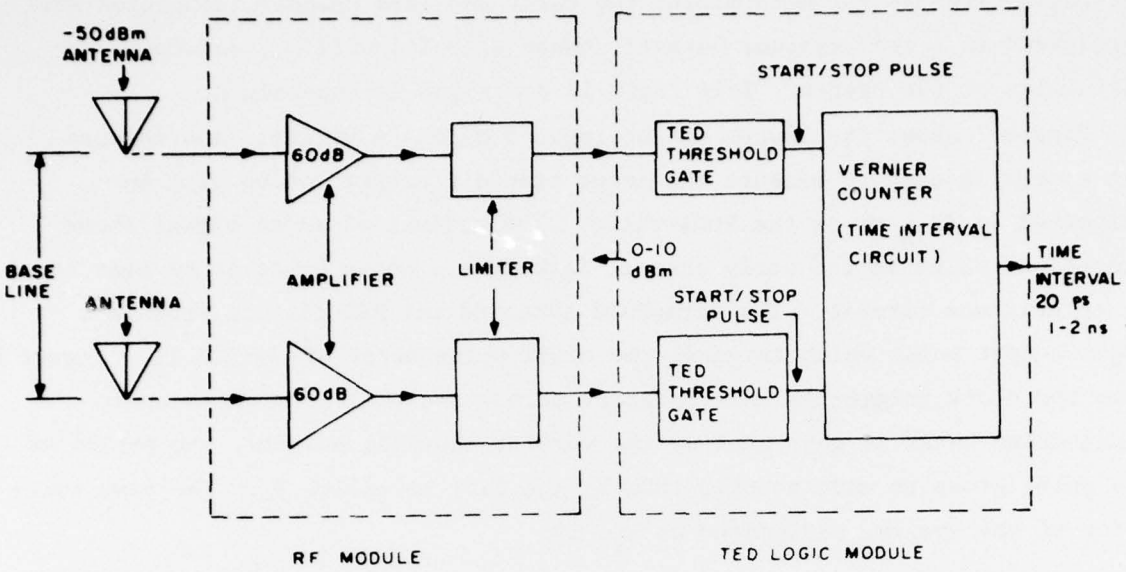


Figure 1. Simplified block diagram of the critical parts of a TDOA system.

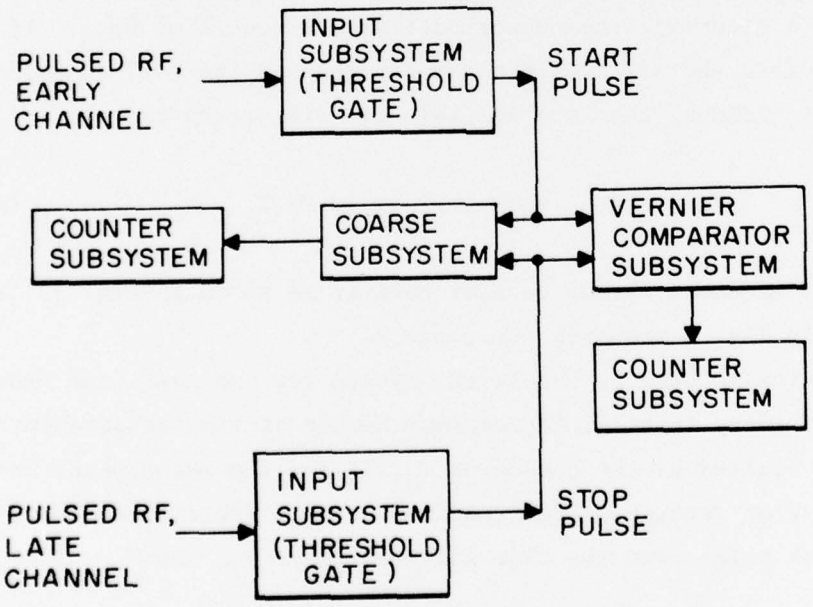


Figure 2. Logic module subsystem.

Logic circuits for determining the early and late channel identities will be required in a real system; however, these circuits will not determine the feasibility of the system. This logic is described in Appendix A.

Figure 3 shows the layout of the logic module. A vernier time measurement system is used to measure the input time difference, which will be designated as Δt_{IN} or as the TDOA value. The arrival of an rf signal above a threshold value at the early channel initiates a pulse burst to be sent to the coincidence circuit. The threshold gate and the SRD circuit produce a single output pulse which triggers the clock pulse burst of period T_C. Figure 4 shows the clock trigger pulse (the start pulse) and the clock pulse train. A second pulse burst is generated by the vernier channel; however, the period of this pulse group is made shorter than T_C and will be called T_V. The time resolution of the system, designated as T_R, is

$$T_R = T_C - T_V \tag{1}$$

When coincidence of the two pulse trains occurs as shown in Fig. 4, the TELD coincidence circuit is triggered and the vernier counter is disabled. This event is used to determine the subperiod time difference of Δt_{IN}. If M clock pulse occurs before the start of the vernier channel and N clock pulses have occurred at coincidence, then the initial time difference is

$$\Delta t_{IN} = (M-1)\ T_C + (N-M)\ T_R \tag{2}$$

The number N is measured by the vernier counter as shown in Fig. 3. The coarse counter shown in Fig. 3 measures the count M.

A reset pulse is used to enable the system for the next time measurement. The measurement rate, that is, the maximum number of time measurements possible each second is limited by the choice of T_C, T_R and the measurement range. Let N_V be the number of vernier pulses required. Since there is one more vernier pulse than clock pulse over the time interval $(N_V-1)T_V$, then

$$(N_V-1)T_V = (N_V-2)T_C \tag{3}$$

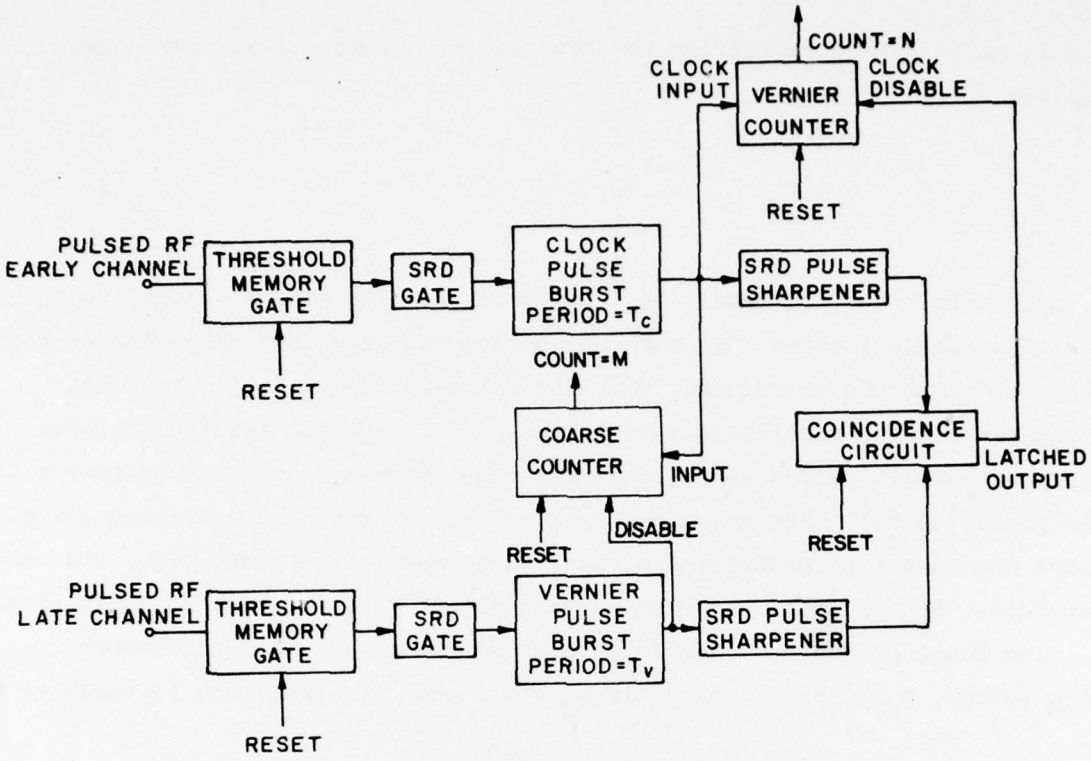


Figure 3. Logic module layout.

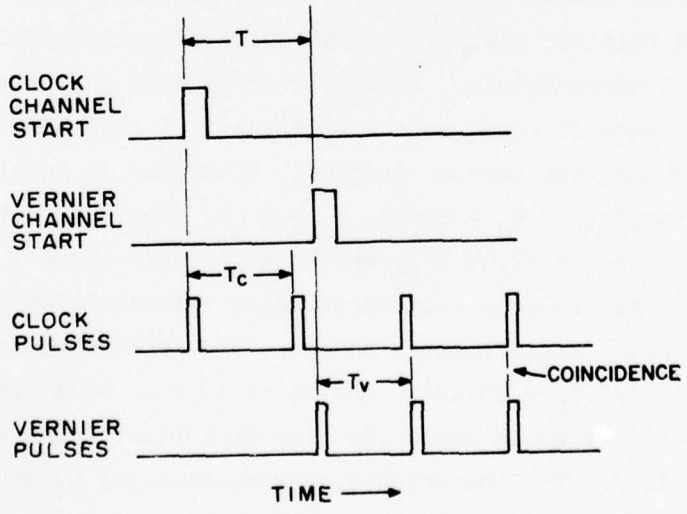


Figure 4. Pulse trains in vernier time measurement system.

This equation can be simplified to show that the number of vernier pulses required is

$$N_V = 1 + \frac{T_C}{T_R} \qquad (4)$$

For good resolution, T_C should be 1 ns, or less. Assuming a nominal value of T_C = 1 ns, Table 1 shows the number of pulses required for each value of resolution and also the measurement time for a time difference of 0 to 1 ns. Notice that a high resolution system, such as T_R = 25 ps, requires a large number of vernier pulses and a long real time interval for the measurement to take place (40 ns). The measurement time for high resolution systems ultimately limits the number of measurements that can be made per second, e.g., the measurement rate. For example, the maximum measurement rate for T_R = 25 ps is 25 MHz.

The range of measurements is simply determined by the total number of clock pulses, N_C. Specifically, if $N_C = N_v$, then the range can be shown to be

$$T_C(2 + \frac{N_C-3}{N_C-1}), \qquad (5)$$

or, between 2 or 3 ns for T_C = 1 ns. This is adequate for the TDOA system with receiver antennas spaced a few meters apart. The stability of the clock's period and the relative stability of the vernier period will determine the useful range of measurements. Baron [2] shows that the permissible clock frequency tolerance is equal to the reciprocal of the coarse interval. Furthermore, he shows that the vernier frequency tolerance is equal to $\pm[2(N_V-1)(N_V-3)T_C]^{-1}$. For example, if T_R = 50 ps, T_C = 1 ns, then $1/T_V$ = 1.053 GHz, and the frequency tolerance is $\pm$1.39 MHz, which is slightly above 1 part per 1000. These requirements are more restrictive than tolerances on an oscillator for a gated time interval measurement. However, the oscillator frequency in such a case could be $\sim$ 1/2 T_R = 10 GHz. Gating of such an oscillator would be difficult.

The half-height pulse width can also be estimated for each value of time resolution desired. For convenience, assume that the pulses are triangular. Figure 5 shows the construction of the sum of two pulses for various values of separation. In this example, each pulse has unity amplitude, and has 100-ps width (at half-height). When the time separation is at least 100 ps, the sum

TABLE 1. MEASUREMENT SPECIFICATIONS AS DETERMINED BY CHOICE OF RESOLUTION, ASSUMING T_C = 1 ns

T_R (ps)	No. of Vernier Pulses (N_V)	Measurement Time (ns)	Pulse Widths Min. (ps)	Max. (ps)
333	4	3	333	667
250	5	4	250	500
200	6	5	200	400
143	8	7	143	286
100	11	10	100	200
67	16	15	67	134
50	21	20	50	100
25	41	40	25	50

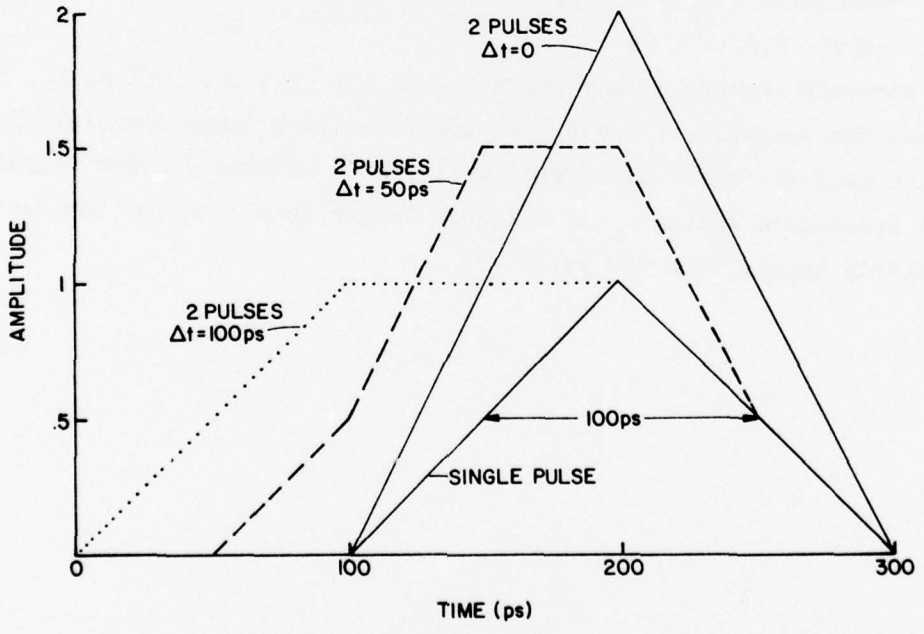


Figure 5. Examples of summing two triangular pulses of half-height = 100 ps.

never exceeds unity. The separation of 50 ps or less assures a sum of 1.5 or more, which is a reasonable threshold condition. For T_R = 100 ps and an actual time difference of 50 ps, the choice of minimum pulse width equal to slightly greater than 100 ps assures triggering of the threshold circuit. On the other hand, if two pulses are 100 ps apart, and T_R = 100 ps, no triggering should occur. This means the maximum pulse width is about 200 ps. Table 1 lists pulse width ranges for each value of time resolution, T_R. Operation within the proper range of pulse width will assure firing of the coincidence circuit.

C. THE BREADBOARD LOGIC MODULE

A breadboard of the logic module has been designed, built, and tested. Since the major objective of this module is to show feasibility of the TELD time interval measurement system, ancillary logic, such as coarse counting and logic to determine the early and late channels (see Appendix A) have been omitted. The following specification were chosen as the goals of the present program:

Clock period = T_C = 1 ns (nominal)

Vernier period = T_V = 0.67 ns (nominal)

Time resolution = T_R = 333 ps

TDOA range: 0.0 to 1 ns

The accuracy cannot be made smaller than the time resolution, T_R, and will depend upon the averaging process used for repetitive input signals. The rf input burst used for tests is several cycles of a nominally 1-GHz signal. In the final breadboard system T_C is slightly larger than 1 ns and the resolution T_R is slightly larger than 400 ps.

SECTION III

EXPERIMENTAL EVALUATION OF THE LOGIC MODULE

A. PRELIMINARY TESTS OF THE INPUT SUBSYSTEM

Figure 6 shows the logic circuits required for pulse train (clock) generation when the input rf increases above threshold. In addition, Fig. 6 shows the voltage waveforms expected at various points in the subsystem for the case of an input rf amplitude above threshold. When the input is below threshold, all subsequent displays should be null displays.

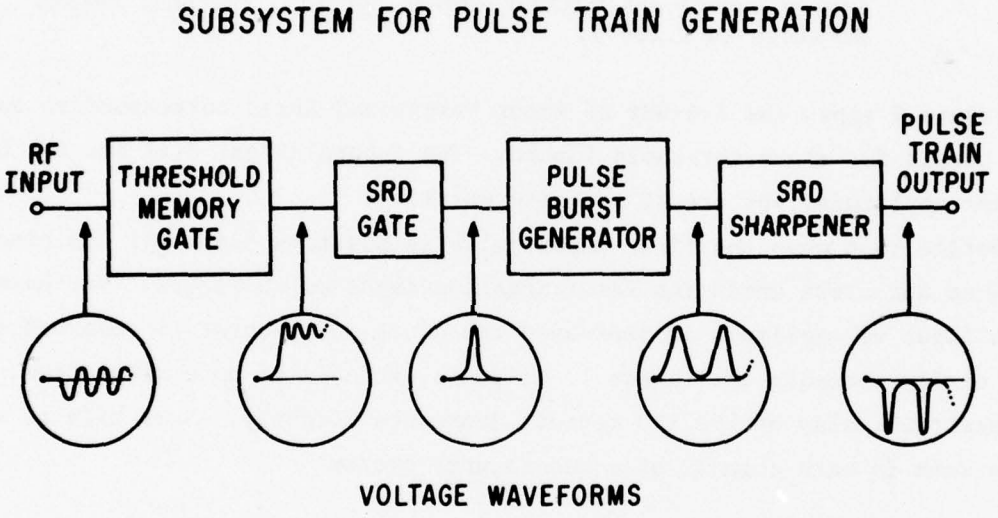


Figure 6. Input subsystem and its voltage waveforms.

An rf burst was used as an input signal for preliminary tests. It consists of two cycles of an 0.8-GHz signal.

Data for clock outputs with a four-pulse (burst) generator, the first SRD circuit and the threshold circuit are shown in Fig. 7. The pulse burst occurs for above threshold input and the null output occurs for below threshold input. The pulse widths must be reduced by the final SRD circuit before being fed to the coincidence circuit.

The input subsystem was tested with an input rf frequency of 1.4 GHz and found to operate as well as with the 0.8-GHz signals previously used. Network analyzer tests showed that the useful input range was below 2.5 GHz due to gate biasing circuitry.

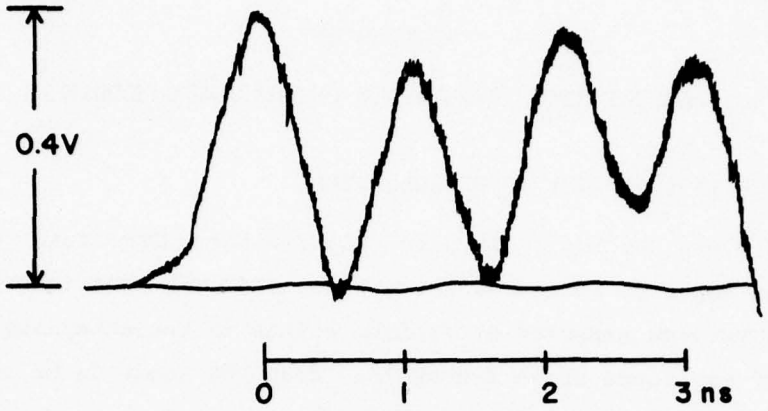


Figure 7. Output of pulse burst generator for peak rf input of 0.272 V (upper curve) and 0.170 V (lower curve). The null output persists to 0.204 V.

Figure 8 shows the 1.4-GHz rf input bursts and their corresponding output clock bursts for above threshold inputs. The inputs (Figs. 8(a) and (b) have the same amplitude, but are of opposite polarity.

Notice that when the first input pulse is positive (input B) the clock pulses do not start until the first negative input pulse occurs. Furthermore, as the input rf amplitude is increased the clock pulse burst is observed to begin earlier because the threshold value is exceeded at an earlier time, and the insertion delay of the SRD circuit decreases slightly. Such effects would be the same in each channel of a two-channel system.

B. FINAL TESTS

Figure 9 is a schematic drawing of the breadboard logic module. All electrical components used in the module are shown except for the power supplies. All the FETs were operated with 5 V on the drain. The input SRD circuits shared one power supply as did the output SRD circuits. A minimum of six power supplies are required. The module is contained on one 16.7 cm x 45.7-cm baseplate. Figure 10 is a photograph of the breadboard module. The relative positioning of the components is almost identical to the layout of the schematic drawing (Fig. 9).

The first tests were made without the two threshold gate circuits. A positive pulse was used as an input to the clock circuit and a second pulse with

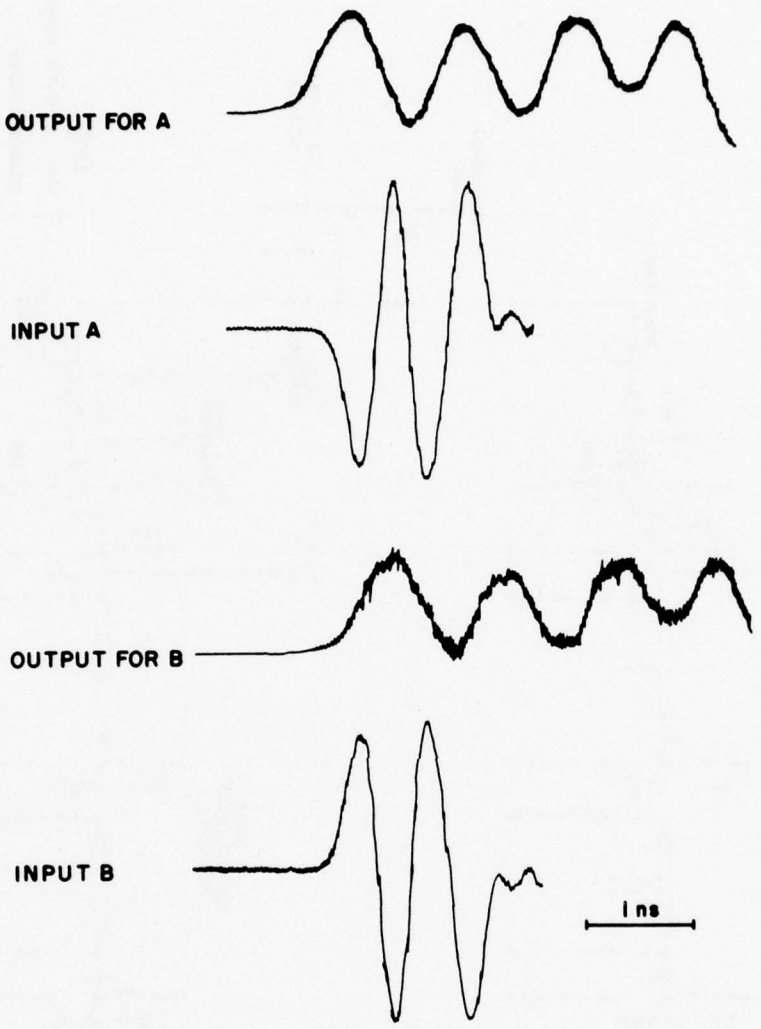


Figure 8. Clock pulse bursts for two different rf inputs at 1.4 GHz. The clock pulse period is 1.1 ns.

adjustable delay was used as an input to the vernier circuit. Pulse values of 0.5 to 0.7 V were used in these tests. Figure 11 shows the clock and vernier channel pulse bursts. The experimental voltage waveforms for the sum of these signals at the gate of the coincidence circuit were also measured. This waveform was measured for vernier channel delays producing coincidence as the first, second, third, and fourth pulses. These are shown on Fig. 12 (a), (b), (c), and (d). The maximum voltage is clearly visible at the proper time in each figure. Notice for coincidence on the fourth pulse, a simultaneous coincidence also occurs on the second pulse. This occurs because $3\ T_R = T_C$ for four pulses

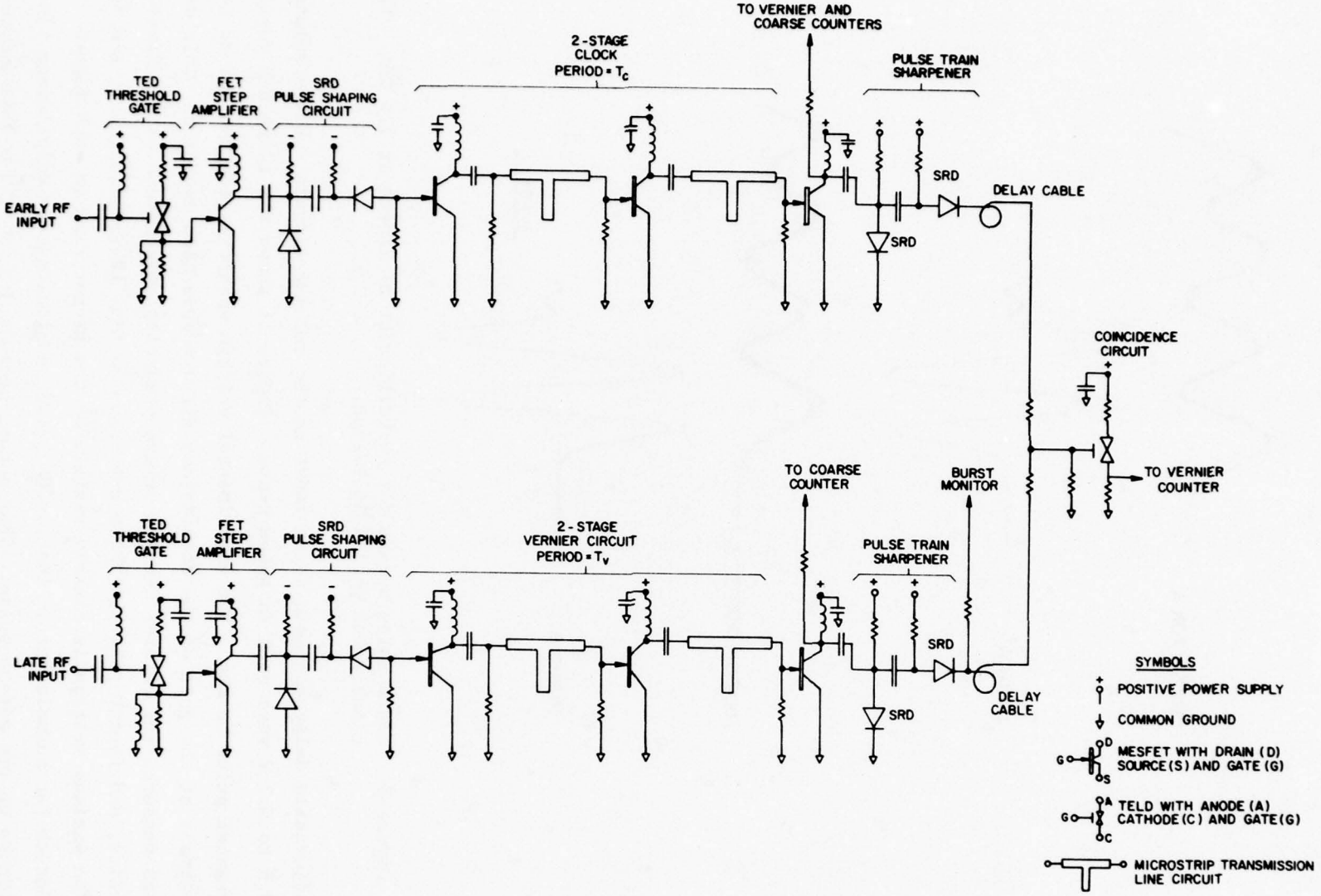


Figure 9. Schematic drawing of breadboard logic module.

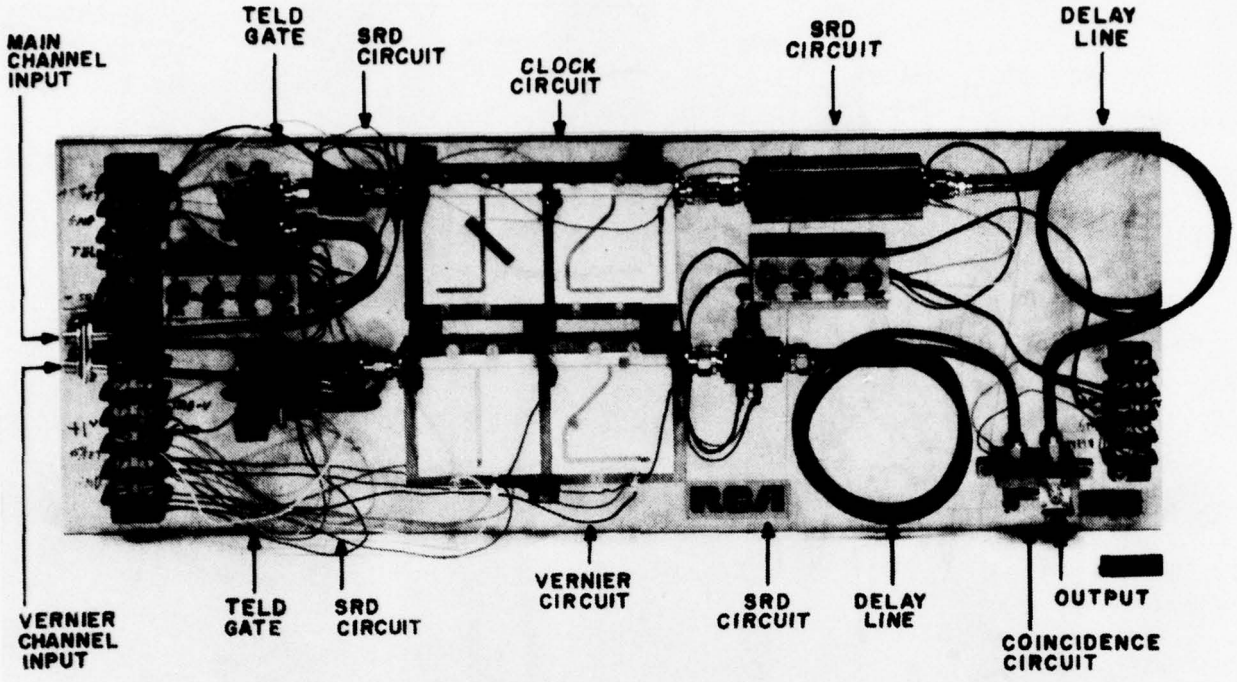


Figure 10. Photograph of the breadboard logic module, as tested.

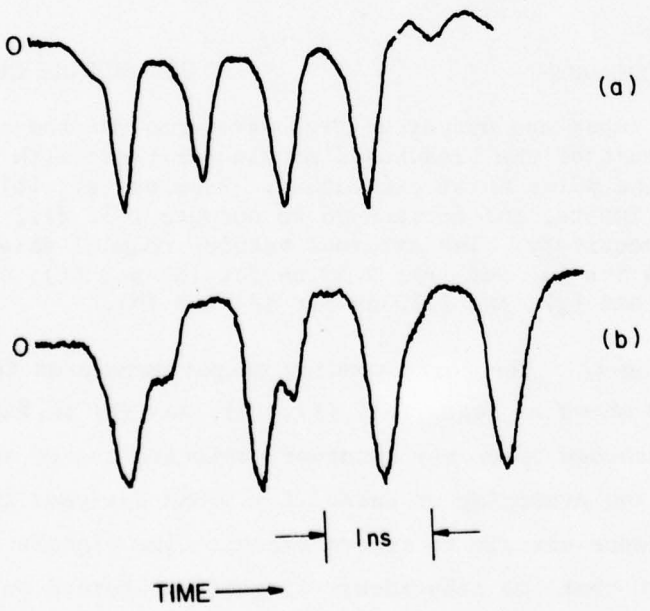


Figure 11. Experimental output waveform for (a) the vernier pulse burst generator and, (b) the clock pulse burst generator.

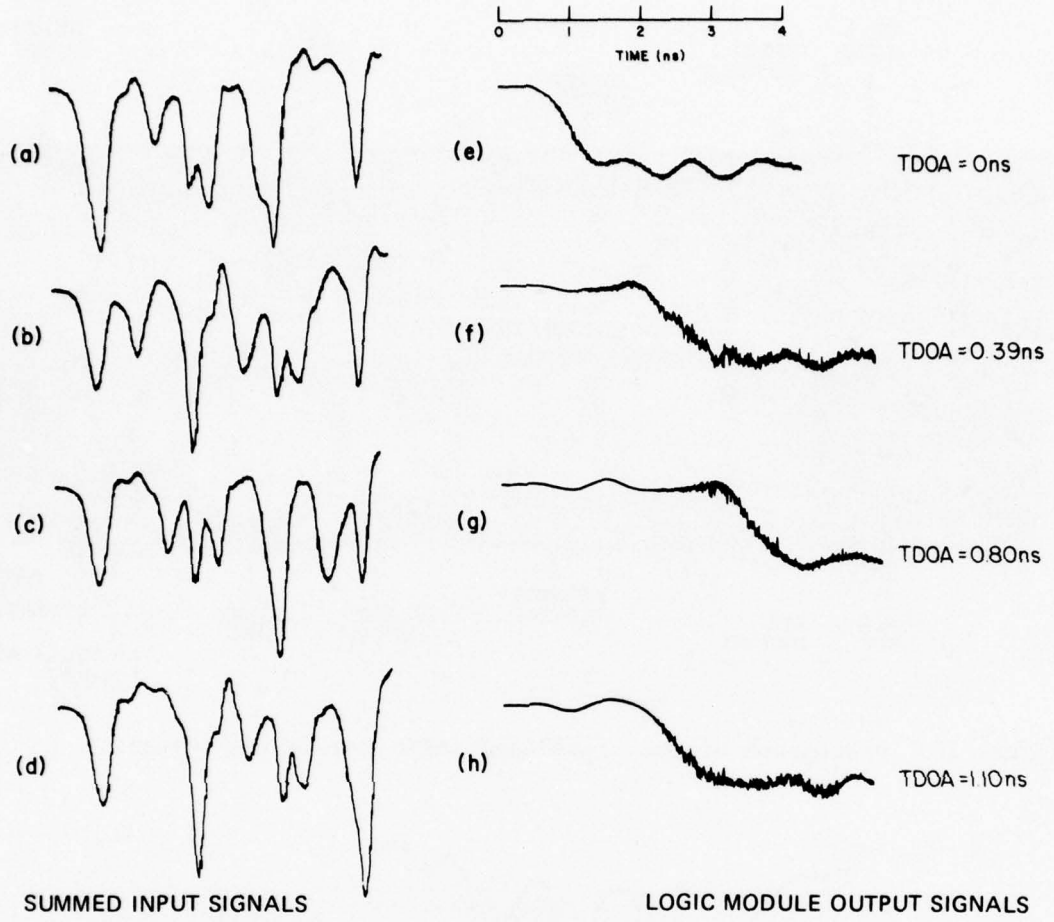


Figure 12. The input and output voltage waveforms for the coincidence circuit of the breadboard module for tests with input pulses to the pulse burst generators. Figures (a), (b), (c), and (d) are inputs, and correspond to outputs (e), (f), (g), and (h), respectively. The external vernier channel delay (TDOA) is 0 ns for (a) and (e); 0.39 ns for (b) and (f); 0.80 ns for (c) and (g); and 1.10 ns for (d) and (h).

(N_V = 4 in equation 4). The corresponding output waveforms for the coincidence circuit are shown as Figs. (e), (f), (g), and (h) in Fig. 12. These waveforms were recorded by an x-y recorder connected to the sampling scope,* and which performed time averaging of data. A 1.5-GHz low-pass filter was used after the coincidence circuit to remove transit-time signals from the output waveforms. Notice that the coincidence circuit has turned on at the proper time in each case. No device adjustments were made during these measurements.

*Tektronix, Inc., Type R561B oscilloscope, Type 3T2 Random Sampling Sweep, Type 3S2 Sampling Unit, Type S-4 Sampling Head (rise time $\leq$25 ps).

Only the delay for the vernier signal was changed. This data clearly shows excellent performance of the two channels and the coincidence circuit.

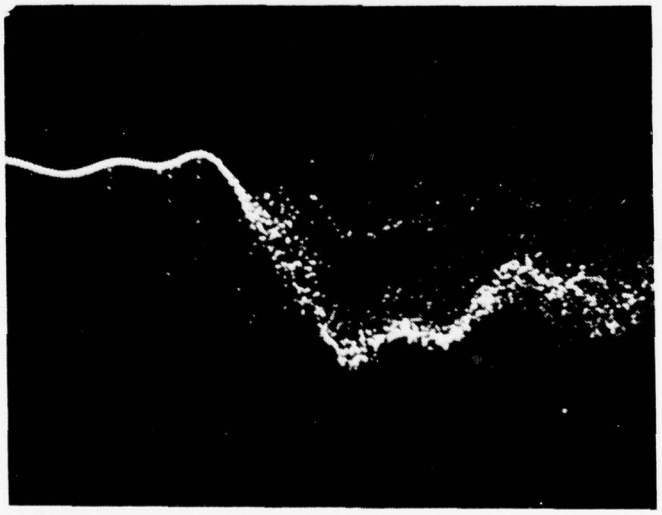
Figure 13 shows photographs of the output waveforms as recorded directly on the sampling oscilloscope. These data were taken at a different time but are very similar to the data for which the x-y recordings in Fig. 12 were made. The noise or fluctuation of data samples can be seen in these photographs. However, each picture contains about 2500 samples (i.e., tests) and the number of improper data points is quite small, i.e., less than 1%. This is the reason for good definition of line in Fig. 12. Figure 14 shows an example of the output data for time delays between 0 and T_R, where $T_R \sim 0.4$ ns. The data of Fig. 14 (a) would be interpreted as 0 ns and Fig. 50 (b) would indicate T_R ns, as desired. This shows proper tranference to digital data.

It was found that the "noise" present in the output waveform of the coincidence circuit increased as the signal amplitude to its gate was reduced. The complete logic module produced slightly less signal at the gate of the coincidence circuit and this is one reason for more noise in the output waveform.

Tests of the complete module were also performed. Figure 15 shows the equipment layout. In these tests the input used was two cycles of an 0.8-GHz rf signal with an amplitude of about 0.4 V. The actual pulse bursts for the clock and vernier channels are shown in Fig. 16. There is slightly more gain in the clock channel and this produces a larger amplitude pulse burst.

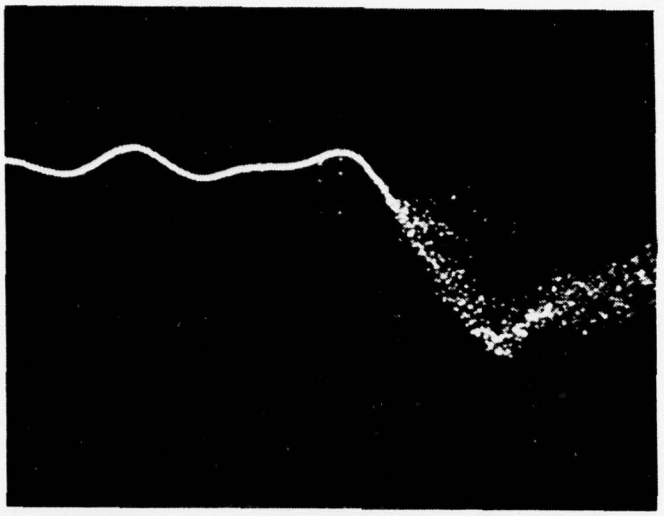
The performance of the whole module is illustrated in Fig. 17. Here, as in Fig. 12, the waveform at the input and output of the coincidence circuit is recorded for four values of delay of the input signal to the vernier channel. The final output step is about 0.25 V into the 50-Ω scope. There is more noise apparent in these waveforms than in the data of Fig. 12. Nevertheless, it is clear that the output voltage steps are occurring at the proper time to properly inhibit the vernier counter. The photographic data for the complete system is generally similar to Figs. 13 and 14, however, there is definitely more "noise." Figure 18 shows a typical photograph for the complete breadboard module and should be compared with Fig. 13 (b).

(a) 0 ns

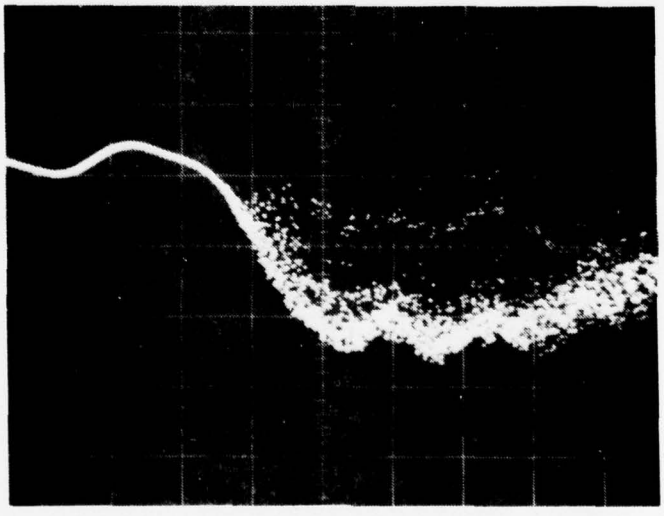


(b) 0.42 ns

Figure 13. Photographs of the output voltage of the coincidence circuit for input pulses to the pulse burst generators. (Vertical scale is 0.1 V/div and horizontal scale is 0.5 ns/div.) The TDOA is noted.

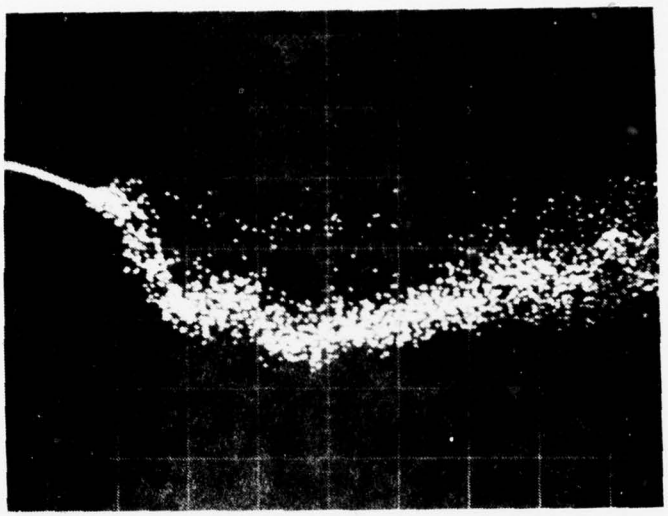


(c) 0.78 ns

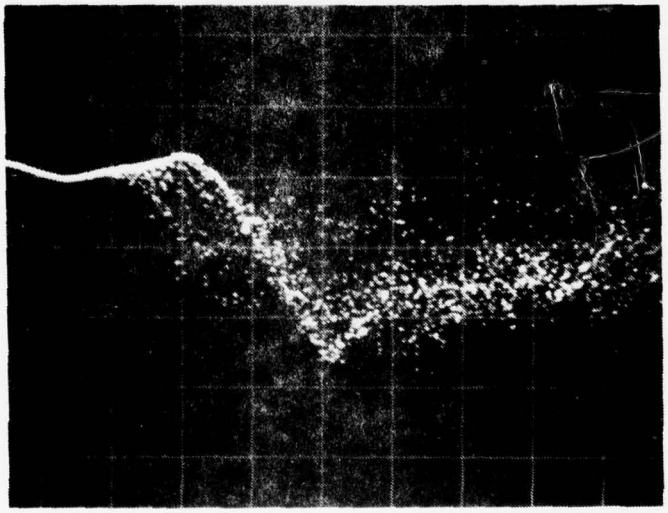


(d) 1.12 ns

Figure 13. (continued)



(a) 0.18 ns



(b) 0.32 ns

Figure 14. Photographs similar to Fig. 49, but for different values of TDOA.

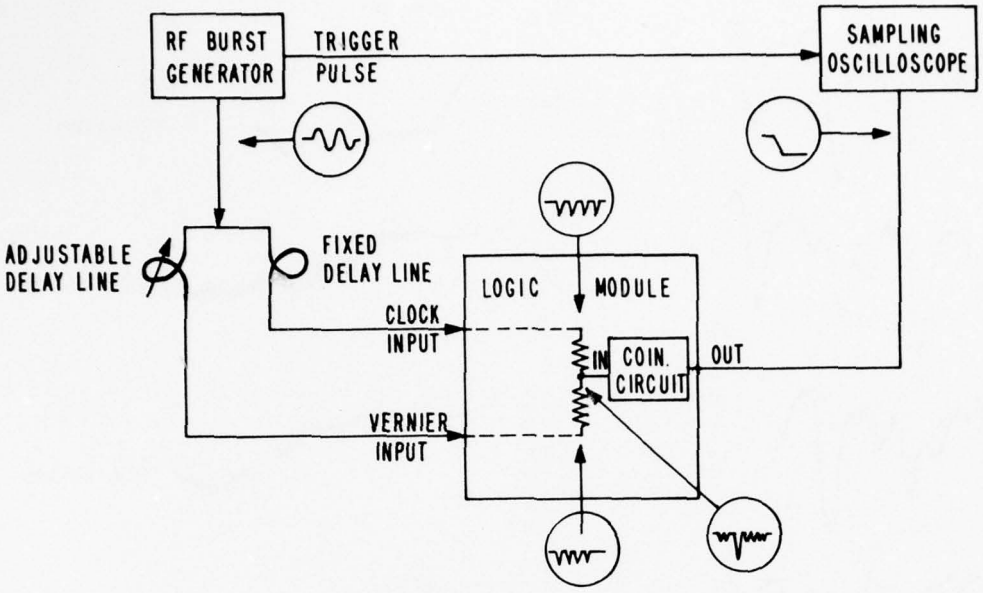


Figure 15. Layout of test equipment for breadboard logic module.

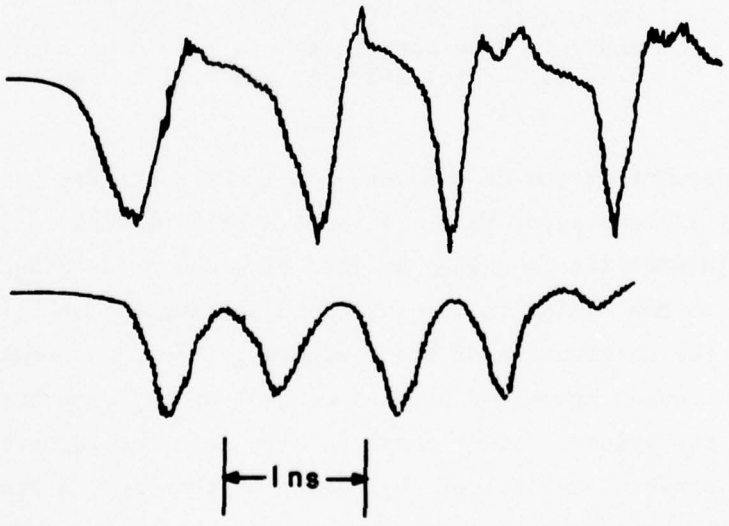


Figure 16. Clock (upper) and vernier (lower) channel pulse bursts in breadboard logic module.

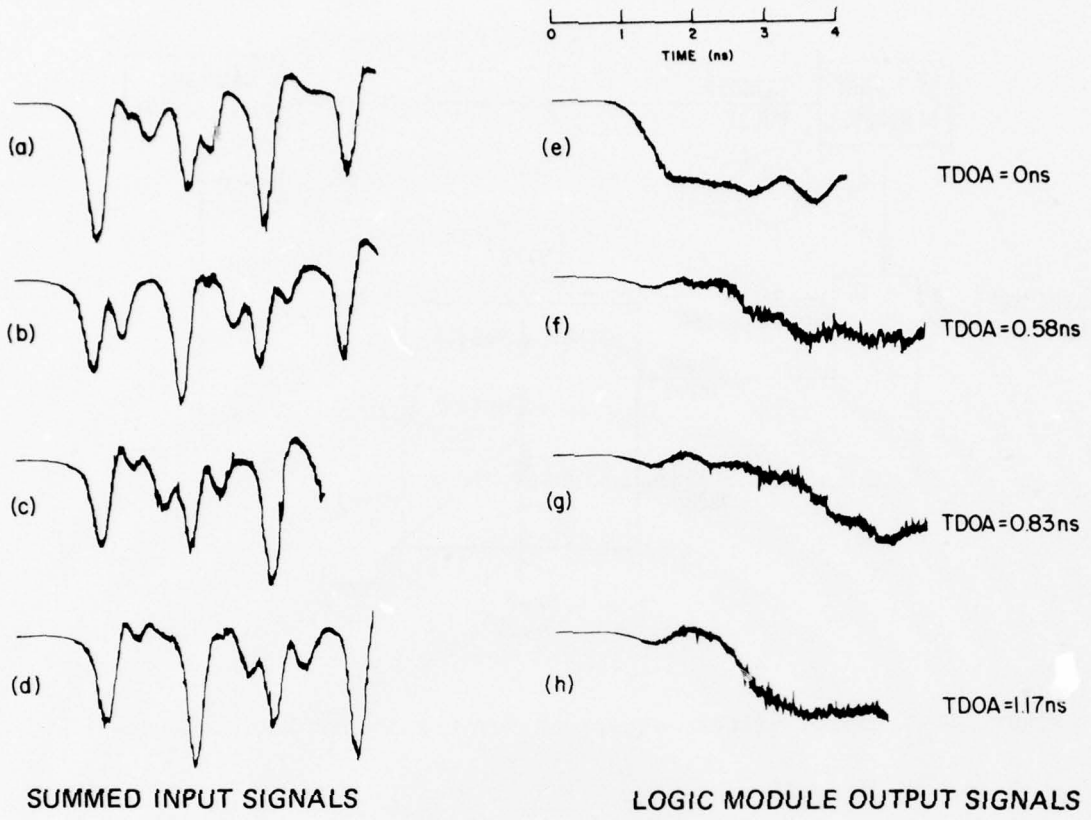


Figure 17. The input and output voltage waveforms for the coincidence circuit of the breadboard logic module with rf inputs. Figure (a), (b), (c), and (d) are inputs and correspond to outputs (e), (f), (g), and (h). The external vernier channel delay is 0 ns for (a) and (e); 0.58 ns for (b) and (f); 0.83 ns for (c) and (g); and 1.17 ns for (d) and (h)

The adjustment of the dc bias on each input threshold gate was critical for obtaining a clear pulse (i.e., without noise) to send to the pulse burst generator. In addition, a change of gate bias causes a change in delay through the gate due to the change in the threshold setting for the rf input signal. This affects the calibration of the equipment. For these reasons it would be desirable to provide means for precise control of the threshold condition of each TELD in the system. Since there is also need for logic to decode the counters and perform statistical evaluation of the data, a good choice for performing all these operations is a microprocessor-based (μP) system. The microprocessor can perform the logic function in a straightforward manner.

Figure 18. Photograph of output waveform of coincidence circuit for test condition similar to Fig. 17 (f). (Vertical scale is 0.1 V/div. and horizontal scale is 0.5 ns/div.)

However, a microprocessor system for controlling the TELDs without interfering with system operation is unusual. Such a system has been devised and is described in some detail in Appendix B. This system could be implemented with commercially available components and would permit proper operation of the logic module by an inexperienced operator.

SECTION IV

COMPONENTS OF THE LOGIC MODULE

A. THE THRESHOLD GATE

1. A Simple TELD Gate

The TELD threshold gate circuit shown in Fig. 19 was constructed with a 35-μm TELD. Microstrip transmission lines were used for the input and the output. The input signal goes to an unpackaged TELD with a thin-film anode resistor of value about equal to the device's low-field resistance. A number of tests were made with the rf burst shown in Fig. 20 as input signal.

Figure 21 shows output waveforms for the threshold gate with $R_C C_C$ = 1 ns. Figures 21 (a) and 21 (b) are the output waveforms for input voltages below and above threshold, respectively. Notice that Fig. 21 (a) is a replica of the input signal whereas Fig. 21 (b) shows a drop in the cathode voltage and a transit-time signal (indicating domain transit-time operation). However, because of the relatively large $R_C C_C$ value, it takes well over 1 ns for the voltage drop to occur.

Figure 22 shows above-threshold waveforms for two other values of $R_C C_C$. The fastest turn-on occurs for the lower curve where $R_C C_C \approx 50$ ps. Here turn-on occurs during the first negative swing in input rf signal.

A number of measurements of gate triggering sensitivity were made using the circuit of Fig. 23. A single negative input pulse, of 600-ps half-width was used to gate trigger a 35-μm TELD with R_A about equal to the TELD's low-field resistance (300 Ω).

The data of Fig. 24 shows that the amplitude of the pulse voltage required for triggering is reduced as the gate is made more negative. However, the output pulse broadens to about twice the input pulse width at -1.5-V bias. This effect is not a problem in the input threshold gates, but is undesirable in other gates.

Figure 25 shows the gate pulse height required for the triggered state as a function of anode and gate bias. Notice that the slope is about one-half. This implies that the device's triggering is twice as sensitive to anode voltage as gate voltage which is undesirable. Improvements in device design can improve the gate triggering sensitivity.

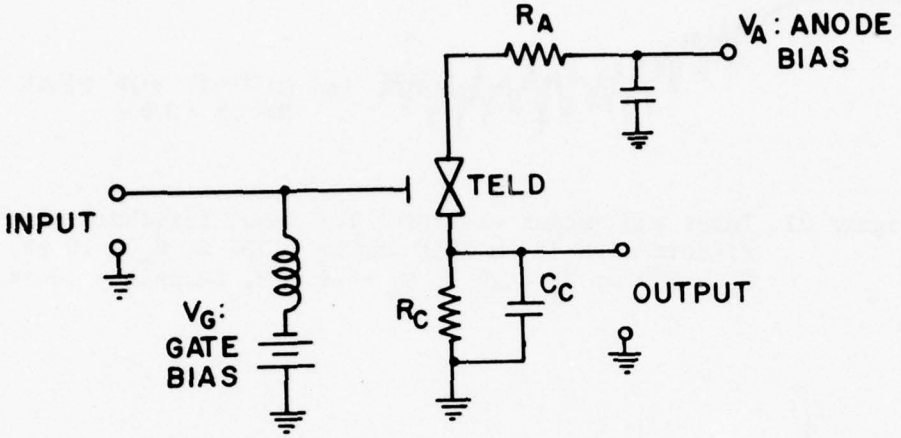


Figure 19. TELD threshold memory circuit.

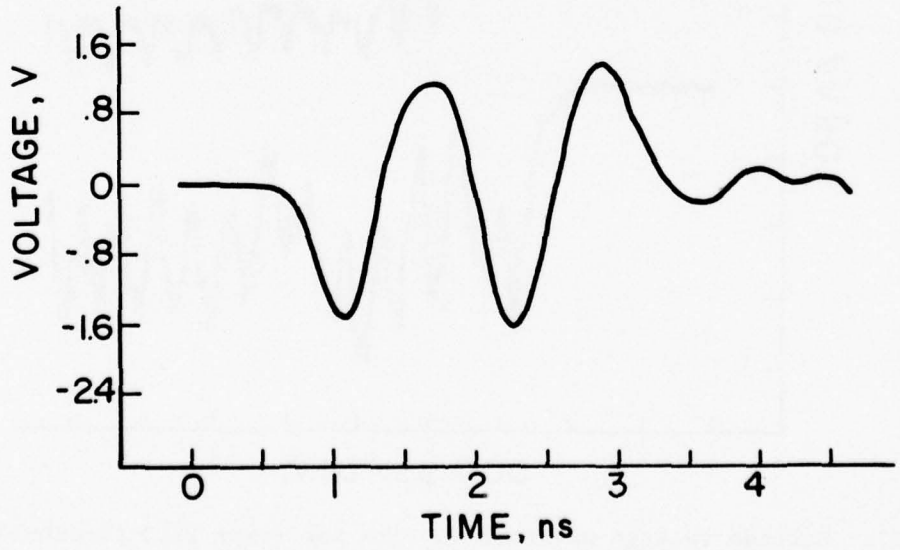


Figure 20. Input rf burst.

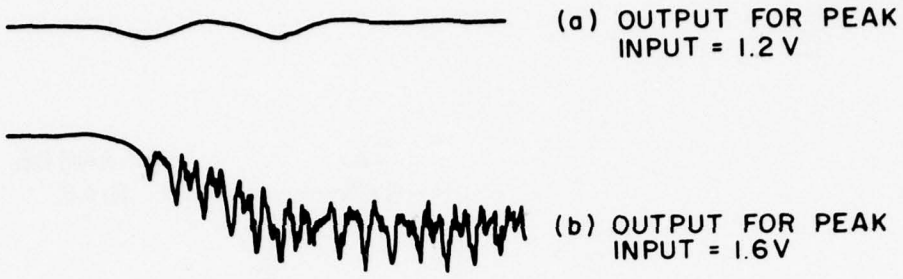


Figure 21. Input and output waveforms for input threshold memory circuit with 35-μm TELD and R_C = 100 Ω, C_c = 10 pF, R_A = 300 Ω, V_A = 19 V, V_G = -0.2 V, Current = 30 mA.

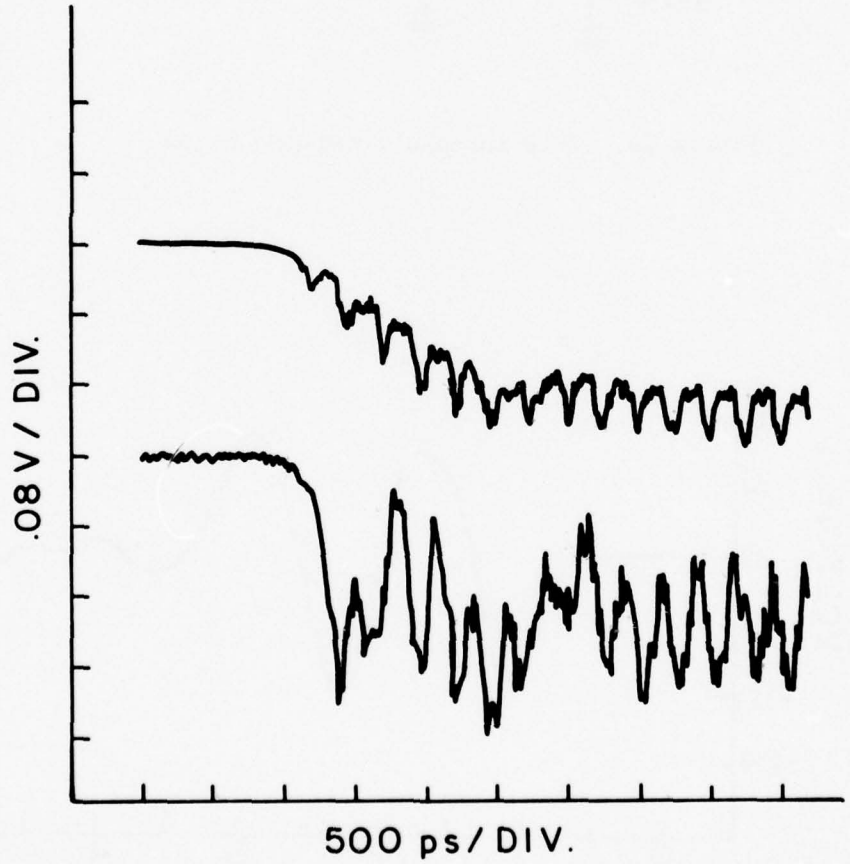


Figure 22. Cathode voltage waveform vs time for 35-μm TELD threshold gate for RC values of 500 ps (upper) and 50 ps (lower) and for a peak input signal of 1.6 V.

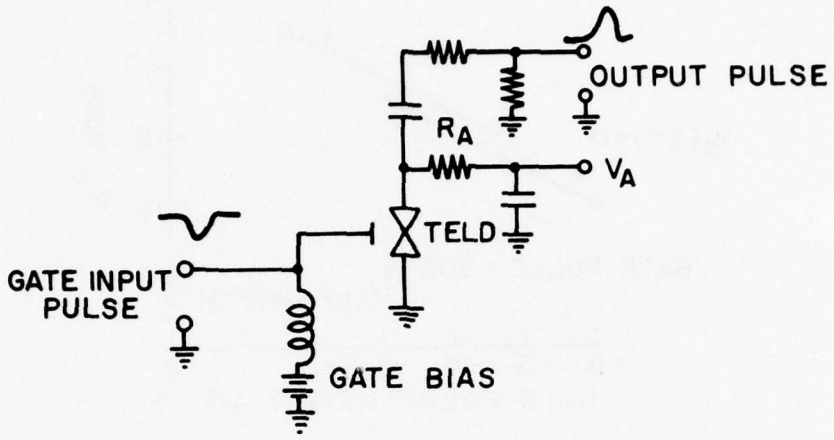


Figure 23. TELD threshold circuit.

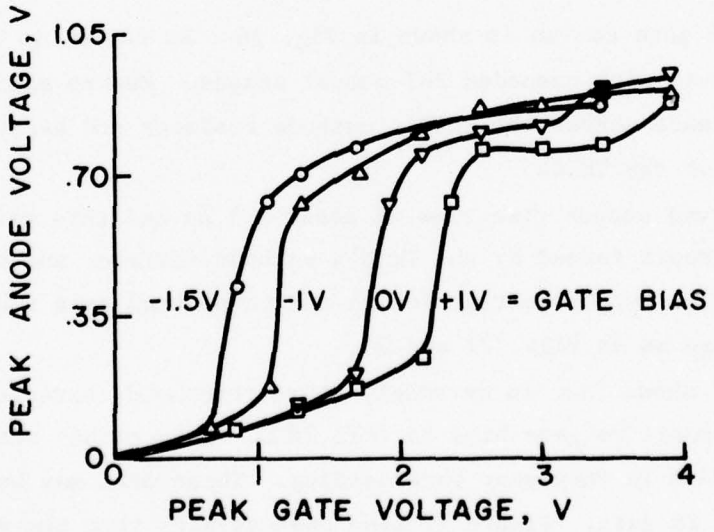


Figure 24. Peak anode voltage vs peak (negative) gate voltage for different gate bias values for 35-μm TELD in circuit of Fig. 10.

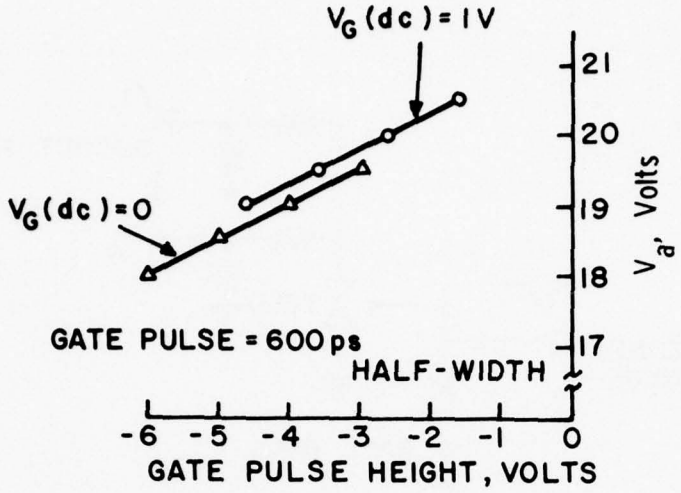


Figure 25. Gate pulse height for triggered state condition as a function of anode voltage for threshold gate with R_A = 300 Ω.

2. Breadboard Design

The final gate design is shown in Fig. 26 As shown, it is basically a threshold circuit with cascaded FET output stages. Memory action occurs because of the capacitance across the TELD's cathode resistor and because of the elevated anode biasing of the TELD.

The observed output rise time is about 0.5 ns and this results primarily from the RC circuit formed by the TELD's cathode resistor and the FET's gate capacitance. The output voltage (step) may be plotted as a function of peak input rf voltage as in Figs. 27 and 28.

Figure 27 shows that an extremely sharp threshold characteristic can be obtained with positive gate bias on this TELD. Notice that zero gate bias (Fig. 28) results in very poor thresholding. These data may be due to some leakage in the SB gate. Figure 27 also demonstrates that the value of (TELD) anode bias controls both the gate gain and gate threshold voltage. Thus, the anode voltage must be set and held within a few millivolts.

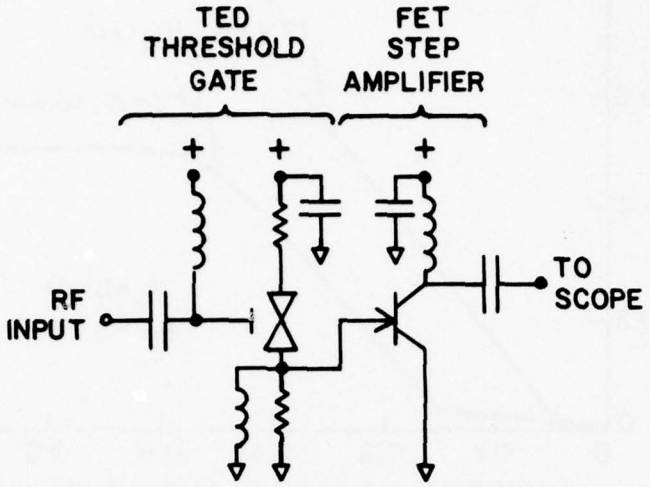


Figure 26. Schematic drawing of the threshold memory gate hardware.

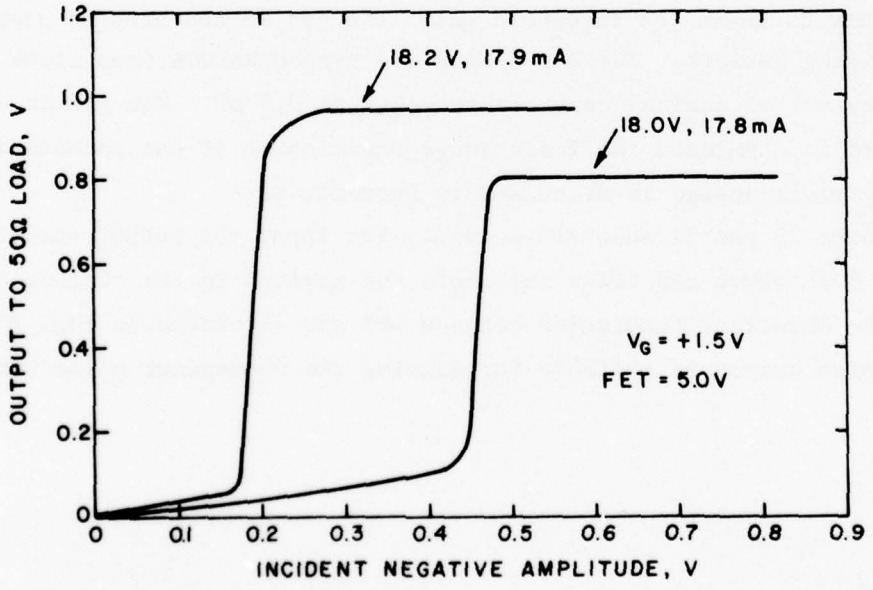


Figure 27. Threshold characteristic for circuit TM3 in memory mode with sine wave input (approximately 0.8 GHz).

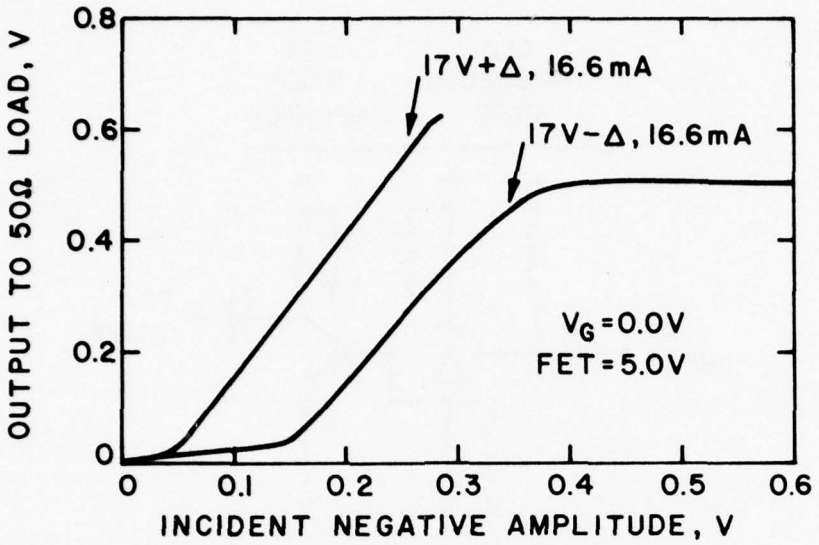


Figure 28. Threshold characteristic for circuit TM3 in memory mode with sine wave input (approximately 0.8 GHz).

Figure 29 shows the threshold gate attached to the step recovery diode (SRD) pulse shaping network. The SRD diodes are type DVB6100A from Alpha Industries, Inc. They are of nominal capacitance equal to 0.5 pF. The series diode is unpackaged to eliminate the feedthrough capacitance of the package (about 0.3 pF). The SRD circuit design is discussed in Appendix B.

Figures 30 and 31 show respectively the input and output waveform for the rf burst both above and below threshold and applied to the circuit of Fig. 29. Notice the excellent resolution between off and on states in Fig. 31. The single pulse output is suitable for driving the subsequent pulse burst generator.

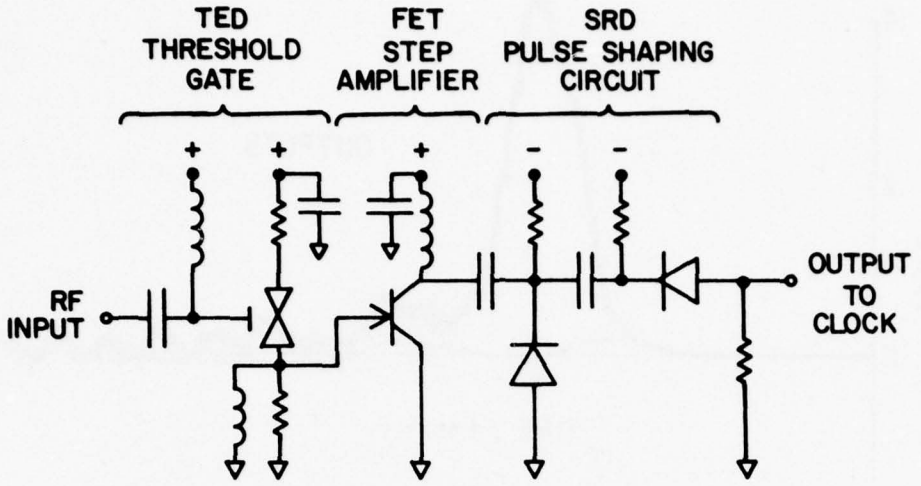


Figure 29. Schematic of threshold gate using a TELD, a GaAs FET and SRDs.

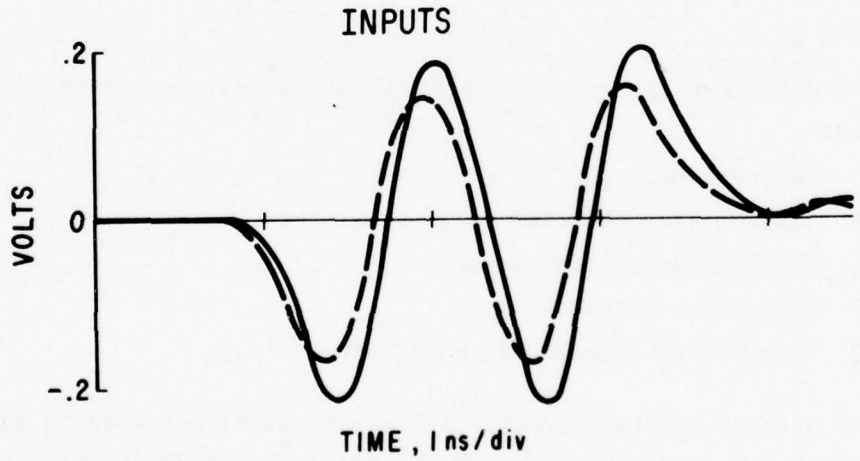


Figure 30. Two amplitudes of rf inputs into the threshold memory circuit.

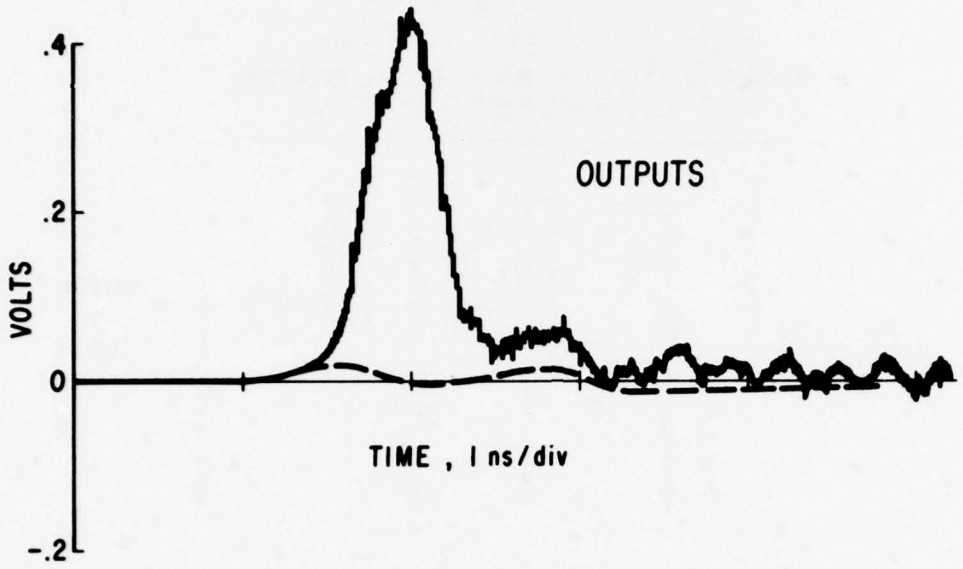


Figure 31. Outputs of the threshold memory circuit for the two inputs of Fig. 30.

B. PULSE BURST GENERATORS

1. Types

Five different designs of clock generators have been constructed and evaluated:

(1) Two-terminal TED
(2) Transmission line/FET pulse generator
(3) FET-TELD pulse regenerator
(4) TELD pulse regenerator
(5) Triggerable subharmonic oscillator

The first design, the two-terminal TED clock, is illustrated in Fig. 32. Here, a series FET is used to "switch on" the TED. Figure 32 (b) illustrates that the TED is operated at voltage V_1 until switched above threshold (V_T) to voltage V_2. The output voltage depends upon the current of the TED. This current is

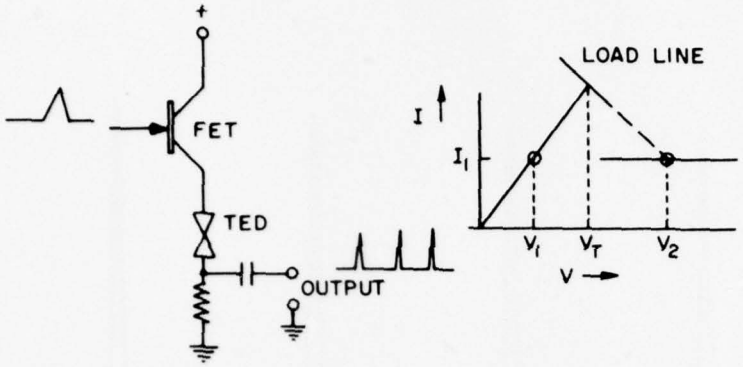


Figure 32. The circuit (a) and current-voltage behavior (b) of the two-terminal TED pulse generator.

the same for both states (V_1 and V_2); however, domain formation current pulses will be observed for voltage V_2. Thus, by using an FET as a switch, the two-terminal TED can be made to produce a train of output pulses. For 1-ns period, a TED of about 100-μm anode-cathode spacing is required. Since V_T will then be about 33 V, the TED must have small enough current (i.e., small area) to permit dc operation and the FET must be capable of switching voltages of value near 30 V.

A planar TED was designed specifically for pulse train generation. Anode-to-cathode spacing is 100 μm and a tapering of the width by 13% from anode to cathode was incorporated. Devices were made from n/SI GaAs with an epi-layer of 5-μm thickness and $6.5 \times 10^{15}/cm^3$ doping density. Using unpackaged chips we have obtained pulse trains with 70-ps half-height and 1.4-ns period as shown in Fig. 33. While the short pulse width and reduced noisiness are very encouraging, an anode trigger voltage of 30 V and a dc bias of 15 V are required to produce a pulse train with 0-V amplitude between pulses, as shown in Fig. 33. This corresponds to the operating points (V_1 and V_2) shown in Fig. 32. The operation of this type of clock is excellent; however, a suitable device for providing the triggering signal (see Fig. 32 (a)) has not been obtained.

Some tests were made to determine if an avalanche transistor could be used for switching on the TED. A Motorola 2N3507 transistor was mounted in the

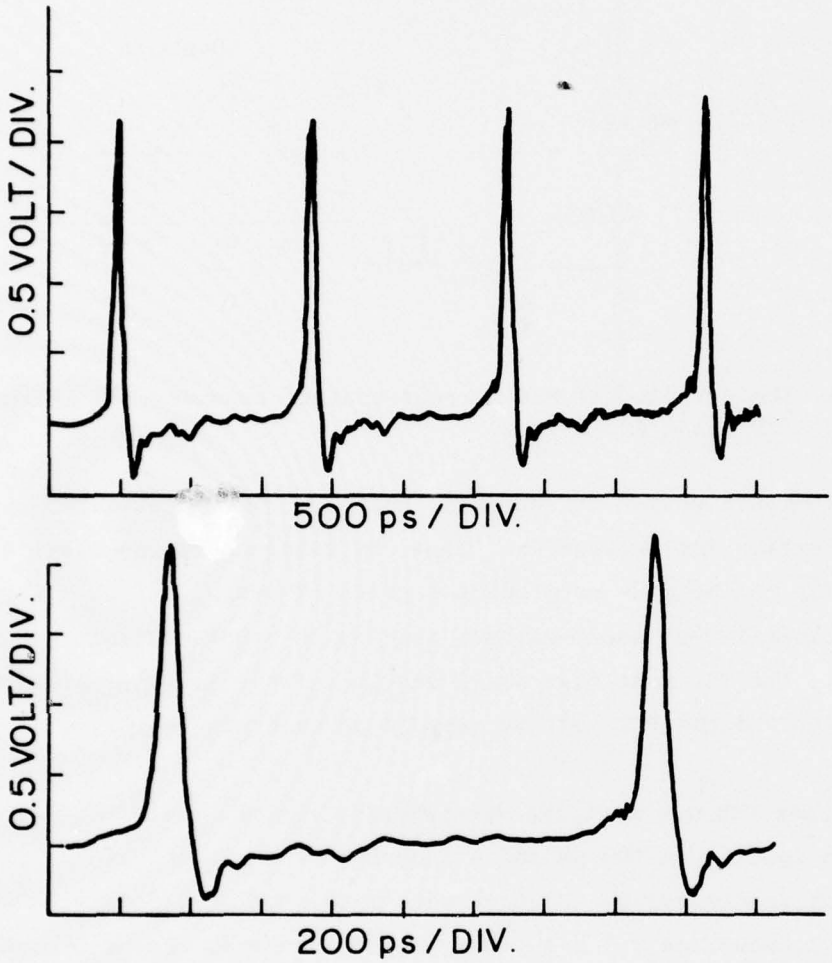


Figure 33. Output voltage waveform across 50-Ω load for two-terminal, tapered TED.

circuit described by Vanderwall, Hattery and Sztankay [3]. It was found possible to switch on a 100-V output pulse with a rise time of 2 ns using a 7-ns, 3-V trigger pulse. However, the minimum delay in the output was 12 ns. In addition, if a shorter input pulse is used, considerable more trigger voltage is required. For example, a 1-ns pulse requires 15-V amplitude for triggering the transistor. Although some of these data can be enhanced with improvements in the

---

3. J. Vanderwall, H. W. Hattery and Z. G. Sztankay, "Subnanosecond Rise Time Pulses from Injection Lasers," IEEE J. of Quantum Electron., QE-10, 570-572 (July 1974).

circuit's design, the triggering requirements and insertion delay are not expected to be improved sufficiently for use with the TED in the logic module.

Figure 34 illustrates the second type of pulse generator. The input pulse is applied to a transmission line T containing an open-circuited section of line length ℓ and one-half the characteristic impedance as the main line. The output of the T section will contain the original pulse (at 1/2 the input voltage) and a second pulse (of the same amplitude) delayed by $2\ell/v$, where v is the velocity of the principal wave on the transmission line. The next T junction will produce four equally spaced pulses from two input pulses by using an open-circuited line of length 2ℓ. The third T junction produces eight pulses in a similar manner. Amplifier stages are placed between the T junction to compensate for the factor of two loss in each junction and to isolate reflections and thus eliminate the need of large delay lines between the T junction. The final pulse train will not have width pulses as narrow as the input pulse due to dispersion in the transmission lines and frequency response problems of the amplifiers. Therefore, a step recovery diode circuit must be used to sharpen the output pulses train.

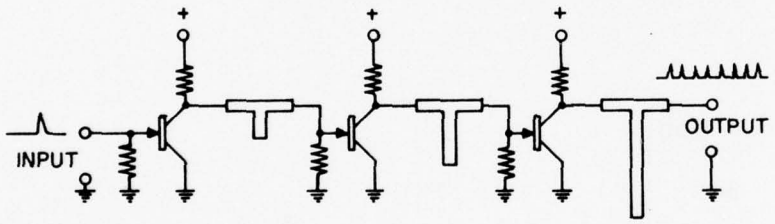


Figure 34. Transmission line FET pulse generator.

There are several problems that must be treated to make this circuit practical. The first difficulty is the amplification stage. No reflections should occur at the input or looking back into the output. Input matching is trivial and the output can be matched by using a load resistance about equal to the transmission line impedance of the output circuit. Since the output loading will probably be about 50 Ω, the g_m of the FET should be approximately 0.04 mmho to produce a voltage gain of 2 (i.e., $g_m R_L = 2$). This large value of g_m is achievable with recent RCA FET designs.

A second problem is the transmission line length of the final stages. To produce 16 pulses, the final stage needs an open line of 4-ns travel time. In alumina substrate microstrip, a line of about 40 cm is required. Fifty-ohm microstrip transmission lines as long as 53 cm have been fabricated on 5-cm (2") square alumina plates in a previous study [4]. Thus, the 40-cm line is realizable.

This design proved to be the simplest to implement within the time scale of this program. It is used in the breadboard design. Figure 35(a) shows a

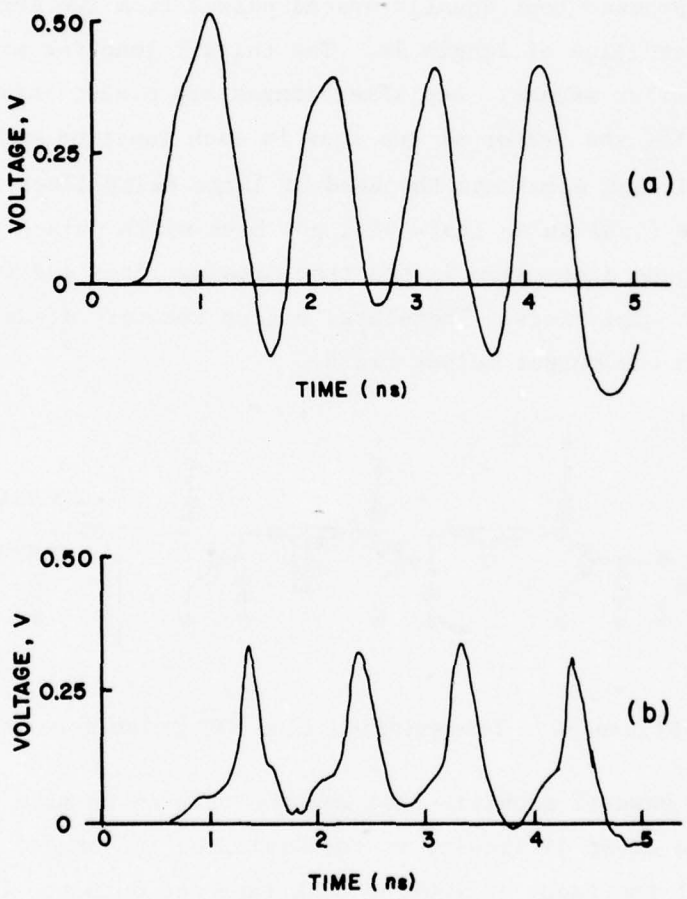


Figure 35. Output of transmission-line/FET pulse burst generator without (a), and with (b) SRD pulse sharpening.

---

4. W. R. Curtice, *Microwave Frequency Memory Using GaAs Transferred Electron Devices*, Interim Tech. Report, Office of Naval Research, Contract No. N00014-74-C-0731, (December 1974).

typical output waveform for a four-pulse burst generator, starting with an input pulse of half-height equal to 250 ps. Notice that the pulse width has been broadened to about 500 ps. This results from the large RC time constant in the gate circuit of the FET devices. The use of the SRD pulse sharpening circuit permits the reduction of the output pulse width, with some sacrifice in amplitude. Figure 35 (b) shows the output of the SRD circuit upon the application of waveform 35 (a). The scales are the same in both figures.

Figure 36 shows the output waveform for a three-stage circuit with SRD pulse sharpening. The period is 1.1 ns and the amplitude of the first pulse is 0.4 V. The net insertion loss is about 5.5 dB since the input pulse amplitude is 0.75 V. The period uniformity is excellent although the pulse height varies appreciably. The maximum pulse width at half-height is 225 ps which is acceptable for an eight-pulse group.

Figure 37 shows a pulse regenerator circuit that is triggered by an initial (input) pulse and stopped by a voltage step. The circuit essentially recirculates the original pulse, using an external delay line to assure that a period of 1 ns is obtained. The first TELD functions as an amplifier and inverter, and the second device is anode-triggered and produces a short current drop (i.e., for 100 ps) so that the output pulse width is short. The advantages of this circuit are: (1) the ease of starting and stopping the pulse train, and (2) the accuracy of the period is excellent, due to the use of the fixed delay line.

A number of experimental circuits were constructed based upon the designs shown in Fig. 37. Two TELDs were used in one circuit. Since this resulted in insufficient voltage at the second device, all other circuits were constructed using an FET as the first device. Although a considerable improvement in voltage gain was realized, a design has not yet been achieved with the desired first stage gain and large output voltage in the second stage (the TELD). All experimental circuits were constructed with separate anode biasing rather than as shown in Fig. 37.

A 35-μm TELD was used with an unpackaged FET in one circuit. The current drop of the TELD was insufficient to provide enough output voltage to permit recirculation. The best result obtained was an output voltage of 0.2 V with

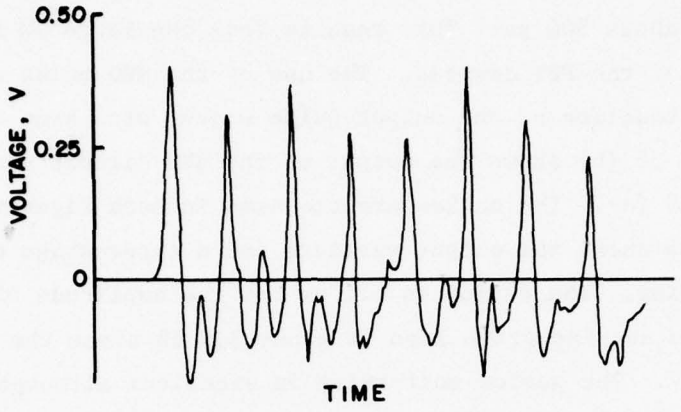


Figure 36. Output of three-stage transmission-line/FET circuit with SRD pulse sharpening.

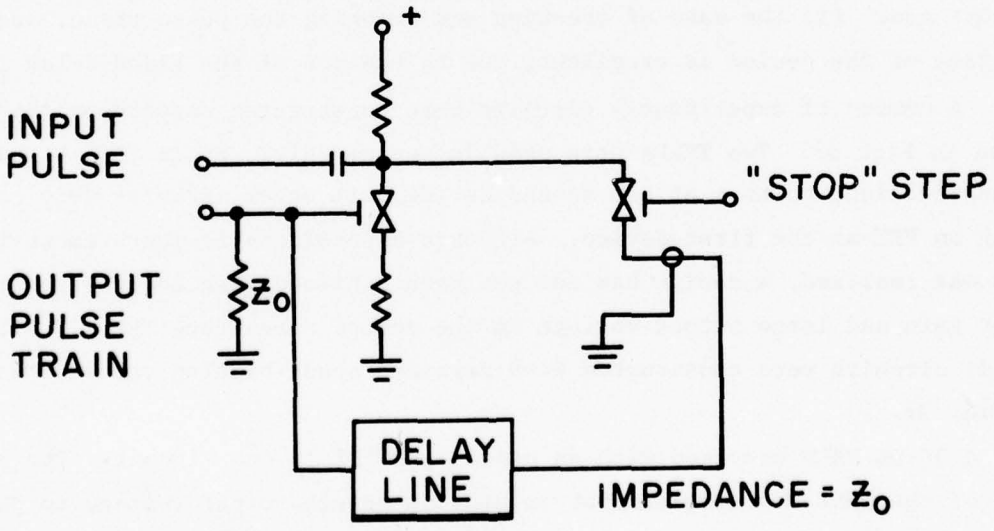


Figure 37. FET-TELD pulse regenerator circuit.

200-ps pulse width for an input voltage of 0.25 V and input pulse width of 600 ps. Figure 38 shows the output waveforms both with and without bias on the TELD for the two stages (without feedback). Notice how the second stage TELD has narrowed the pulse width and inverted the polarity.

The most recent circuit design of this type is shown in Fig. 39. Two 35-μm TELDs were operated in parallel in an attempt to produce large (additive) current drop and a large output signal. Figure 40 shows the pulse trains generated at the output with the feedback transmission line in place. Figure 40 (a) illustrates the case of 0 V on the TELD. Here, the input pulse, which is negative, is sent through the FET which inverts it and it goes through the passive TELD to appear as a positive pulse about 2.5 ns later. A third pulse which is positive, appears after 5.0 ns (2 cycles) and a fourth pulse which is negative, appears after about 7.5 ns (3 cycles). Figure 40 (b) shows that with bias on the TELD, a train of all negative pulse results with the same pulse spacing as in Fig. 40 (b). Therefore, Fig. 40 (b) demonstrates that pulse regeneration by means of this circuit is possible; however, the pulse width and amplitudes are quite unsatisfactory. Improved results can be obtained by using an FET with large g_m and a TELD with larger current drop.

The clock circuit shown in Fig. 41 uses only one TELD. The input pulse can be applied either at the anode (a positive pulse) or at the cathode (a negative pulse). After a domain is triggered by the input, a negative output pulse is produced at the cathode. This pulse travels through the delay line to the output and also causes gate triggering of the TELD to produce the next pulse. In order for this circuit to function properly, the gate triggering sensitivity of the TELD must be good, without biasing the TELD too close to threshold (where memory action can occur).

The clock circuit shown in Fig. 41 was constructed in microstrip using a 12-μm TELD. A positive pulse is applied to the anode that is dc-biased just below threshold. The positive pulse causes domain formation and current drop occurs. The drop in current produces a negative cathode pulse which is transmitted to the gate through the transmission line after a delay of about 0.6 ns. The gate signal causes triggering of the TELD and a new cathode signal is generated. In this manner, a train of pulses is produced at the gate (load) for a single (initiating) input pulse.

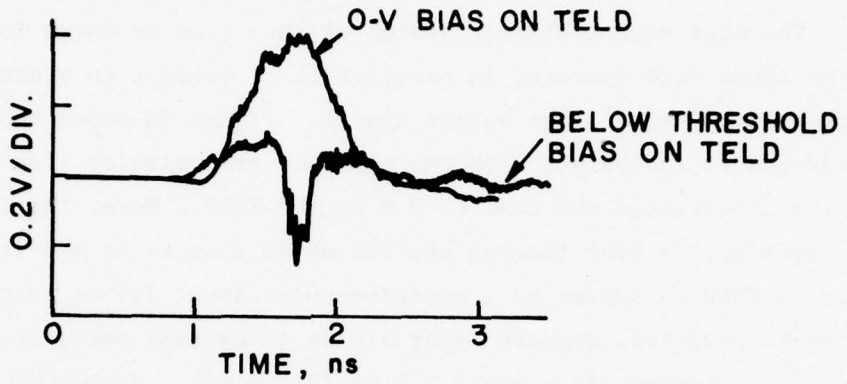


Figure 38. Cathode voltage as a function of time for FET-TELD clock.

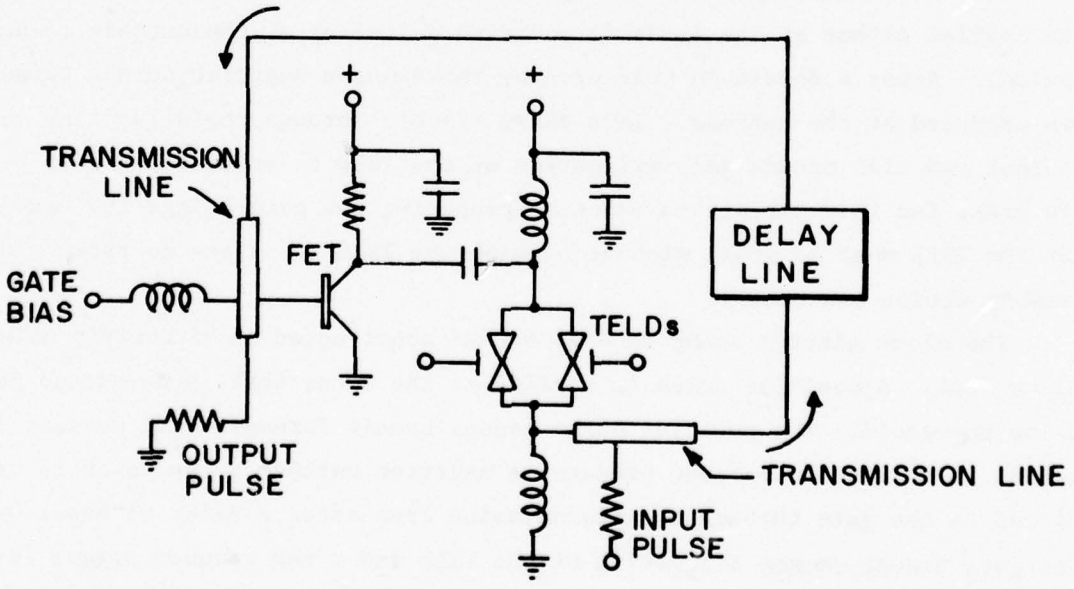


Figure 39. Circuit design of experimental FET-TELD pulse regenerator.

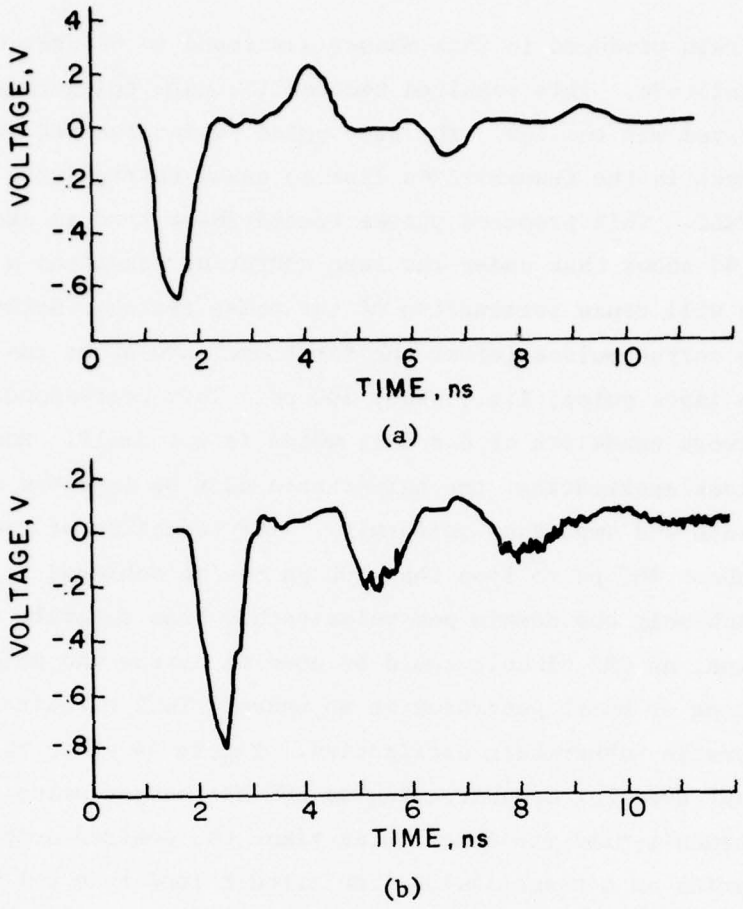


Figure 40. (a) Output pulse train with no voltage on the TELD.
(b) Output pulse train with TELD biased near threshold.

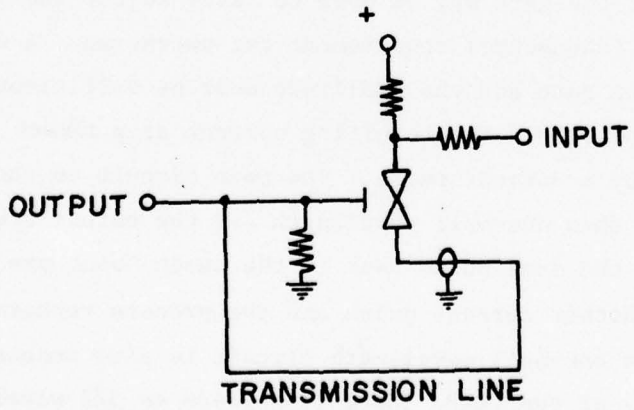


Figure 41. TELD pulse regenerator.

The pulse train produced in this manner was found to be very noisy and of decreasing amplitude. This resulted because the gate triggering sensitivity of the device tested was too low. The best pulse train observed was produced by using a mismatch in the transmission line to cause retriggering at the cathode of the TELD. This produced pulses spaced about 1 ns as shown in Fig. 42 (b). Figure 43 shows that under the same operating condition a later negative anode pulse will cause termination of the pulse trains. Notice that the rise time of the output pulses (after the first one) are about the same as the rise time of the input pulse; i.e., about 300 ps. This corresponds to a transmission network bandwidth of 6.6 GHz, which is not small. However, to be useful in the clock application, the pulse train must be improved with regard to both pulse width and amplitude uniformity. The reduction of the present pulse width of about 500 ps to less than 100 ps can be achieved by permitting the TELD to launch only one domain per pulse rather than several, as obtained here. In addition, an SRD circuit could be used to narrow the pulse.

The fifth type of burst generator is an unusual TELD circuit designed to produce a triggerable subharmonic oscillation. Figure 44 shows the circuit and device arrangement used for demonstrating an 800-MHz output pulse train.

A TELD of transit-time frequency three times the desired output frequcny is mounted in series on a transmission line circuit less than 0.1 wavelength from the short circuit. The open-circuited transmission line is connected to the anode and the short-circuited section is connected to the cathode. The anode is based to a few tenths of 1 V below threshold value with a dc power supply. DC-biasing of the gate may be used to later adjust the output waveform, but it is not a fundamental requirement for operation. A negative trigger pulse is applied at the gate and the amplitude must be sufficient to cause domain formation in the TELD. The resulting current drop causes excitation of the resonant circuit by a current pulse. The open circuit on the transmission line is slightly less than one-half wavelength (at the output frequency) from the TELD and reflects the same pulse back to the anode about one (output) cycle later. This causes another current pulse and the process repeats. The oscillation will persist since the one-half wavelength circuit is also resonant near the transit time frequency of the TELD. Here it appears as 3/2 wavelength. Thus, the circuit will sustain the third subharmonic signal. This frequency can be changed by

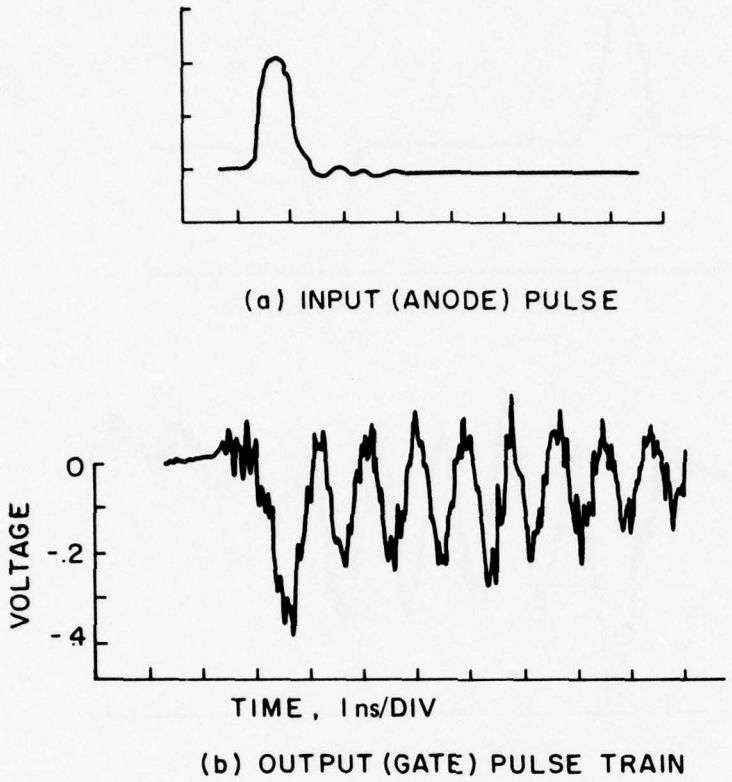


Figure 42. Input (a) and output (b) pulse trains generated by a 12-μm device in TELD clock.

altering the length of the transmission line. The TELD will operate satisfactorily over a moderate frequency range so the harmonic relation is always maintained as the line length (and fundamental frequency) is changed. The output signal is taken from the cathode to another transmission line. A resistor is used here to decouple the output load so as not to interfere with the resonant circuit.

Several different output waveforms have been obtained. Best viewing is achieved by using a low pass filter to remove the transit time frequency. A copy of the pulse train output (at 800 MHz) produced by a 35-μm TELD, triggered on with a 0.7-ns input pulse is shown in Fig. 45.

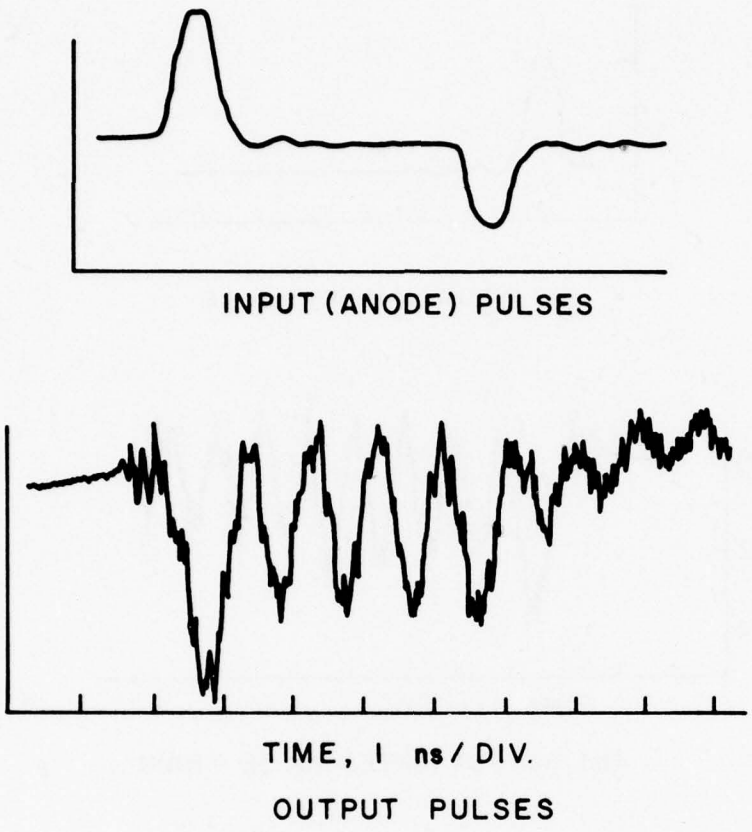


Figure 43. Waveforms for TELD clock (with stopping pulse).

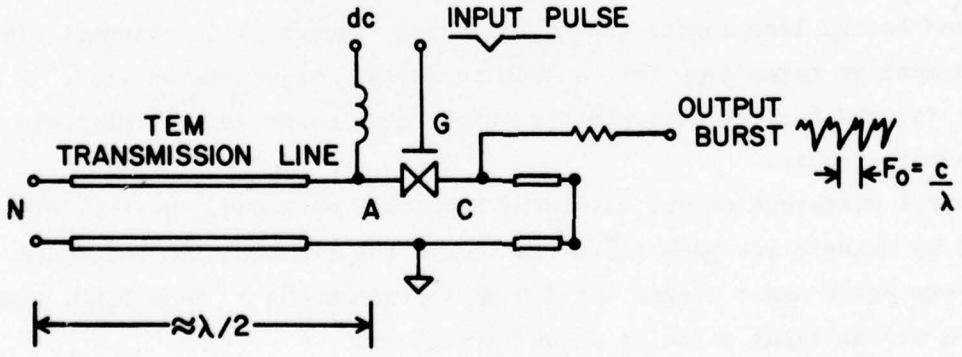


Figure 44. The experimental circuit of the triggerable TELD subharmonic oscillator.

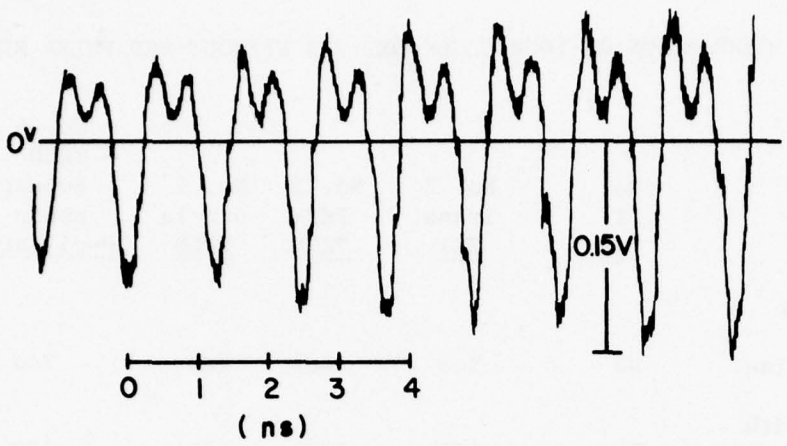


Figure 45. Output voltage waveform of the triggerable TELD subharmonic oscillator.

The pulse train shown in Fig. 45 is excellent with regard to pulse width and period uniformity. However, a gradual increase in amplitude can be seen in the figure. This results because the TELD is operated too close to threshold bias. Use of some series anode resistance should remove this amplitude change by permitting the TELD to be initially biased further below threshold.

The five different designs of pulse burst generators have been constructed and evaluated. Table 2 presents a comparison of the properties of the experimental circuits. The TED clock is the only clock producing pulse widths of less than 100 ps; however, the TED cannot be triggered-on with present FETs. Therefore, this design should not be pursued in future work. The next best performance is observed from the TELD subharmonic oscillator (No. 5), and this design should be developed further. The FET-TELD pulse regenerator shows great promise, but the circuit implementation must be greatly improved. All the TELD circuit designs suffer from the difficulty that they must be critically adjusted for proper operation. The only circuit suitable for immediate implementation in the breadboard design is the transmission-line/FET design.

TABLE 2. COMPARISON OF FOUR CLOCK DESIGNS WITHOUT SRD PULSE SHARPENING

	No. 1 TED	No. 2 Trans. FET	No. 3 FET-TELD	No. 4 Single TELD	No. 5 TELD Subharmonic Oscillator	Units
1. Turned on with one input pulse	No	Yes	Yes	Yes	Yes	
2. Pulse width (1/2 height)	70	500	1000	600	300	ps
3. Period	1.4	1.0	2.7	1.1	1.2	ns
4. Period uniformity	Excellent	Excellent	?	Poor	Excellent	
5. Amplitude uniformity	Excellent	Good	Poor	Fair	Fair	
6. Size	<1	80 for 8 pulses	<4	<10	<8	cm^2
7. Output amplitude	2	0.5	0.2	0.2	0.15	V

2. Breadboard Design

The clock and vernier channel pulse burst generators were designed as transmission-line/FET pulse burst generators. Two stages were used in each to produce four output pulses. Figure 46 shows a sketch of the breadboard circuit. Each transmission line circuit is 5 cm x 5 cm x 0.125 cm (2" x 2" x 0.050") and made of alumina. It contains a main transmission line of characteristic impedance equal to 92 Ω and a branch transmission line of characteristic impedance equal to 46 Ω. Chip resistors are used to match the ends of the main transmission line and an inductor is used to supply bias to each FET. The FETs have 600-μm gate width and g_m equal to about 35 mmhos.

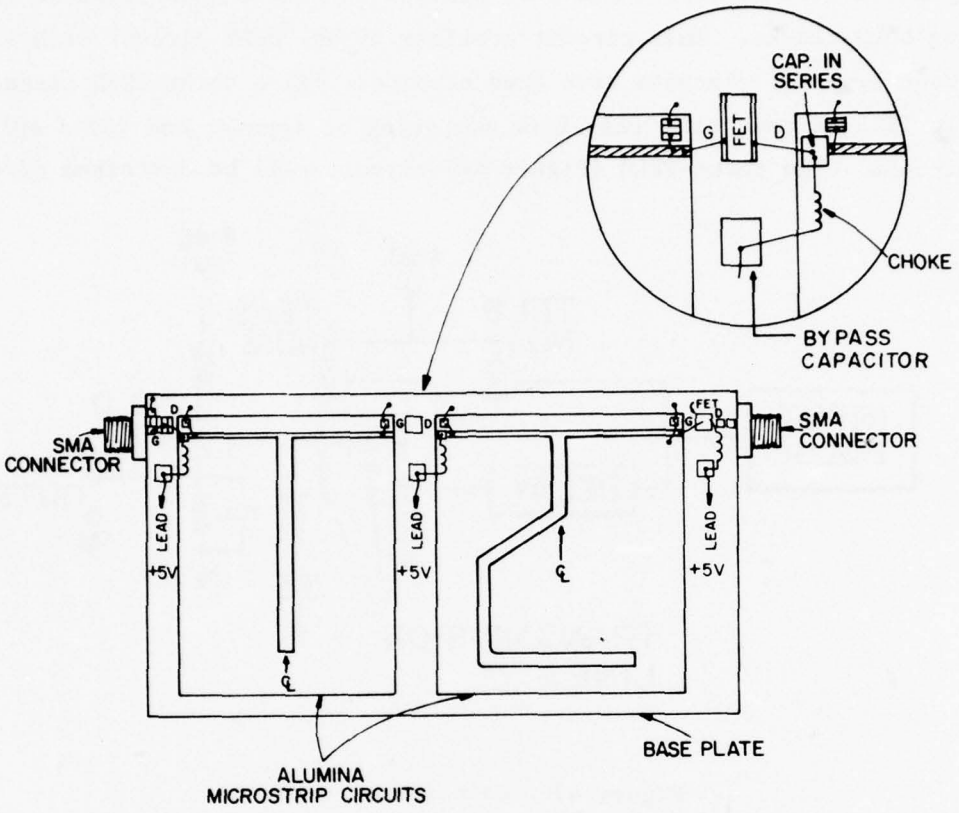


Figure 46. Breadboard layout of the transmission-line/FET pulse burst generator.

The pulse burst generator circuit is followed by an SRD circuit of the same type as shown in Fig. 29. This circuit permits adjustment of the pulse widths. Figure 11 shows the output waveform for the clock and vernier channels of the breadboard circuits. The periods and the system resolution can be found from this data to be: T_C = 1.17 ns; T_V = 0.75 ns, and T_R = 0.42 ns.

C. COINCIDENCE CIRCUIT

1. Design Considerations

The function of the coincidence or "AND" circuit in the TDOA system is to provide an output only when time coincidence has occurred for the two clock generators. As shown in Fig. 3, the coincidence circuit will have the two

clock pulse-trains as inputs and must provide an output step suitable for stopping both clocks. This circuit consists of an "AND" circuit with latching.

Three types of circuits have been studied: (1) a three-TELD circuit; (2) a single TELD circuit with resistive combining of inputs; and (3) a split-gate TELD circuit. The three-TELD (Figure 47) circuit will be described first.

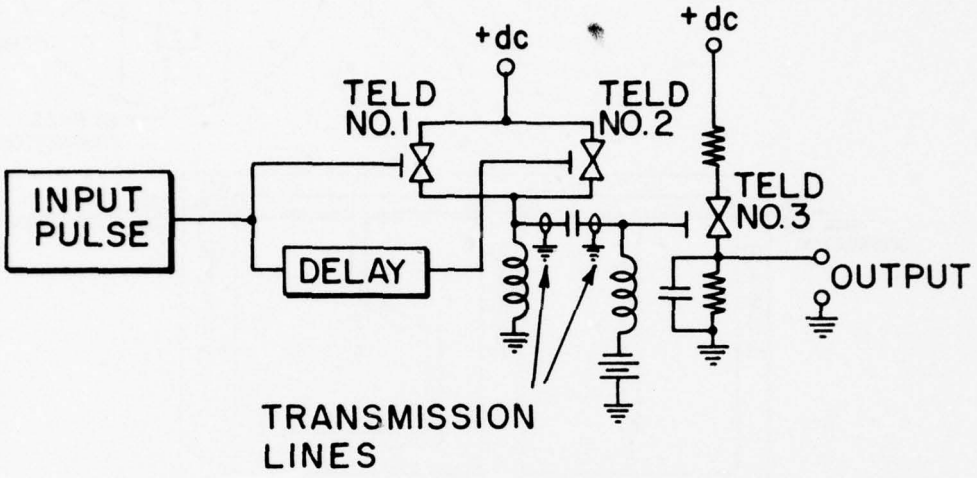


Figure 47. Coincidence circuit.

This first part of the three-TELD circuit consists of two TELDS connected to a common cathode resistor, as in Fig. 48. The gate of the first TELD is triggered by one of the inputs, while the gate of the second device is triggered by the second input. When the two inputs are in time coincidence, a large output voltage is produced, compared to when the inputs are not in time coincidence. The output voltage is then applied to the gate of a TELD threshold memory circuit. The value of the gate threshold voltage of this device is adjusted so that the TELD will be triggered only by the larger output of the previous circuit (i.e., when the two inputs are in time coincidence). This three-TELD coincidence circuit is superior to using one TELD with resistive adding at the gate since it provides superior isolation between the two inputs. This isolation is necessary in a system processing 100-ps pulses.

The circuit shown in Fig. 48 was constructed using packaged 35-μm TELDs mounted in a microstrip circuit. The output waveform across a 50-Ω termination is shown in Fig. 49 for the case of 600-ps (negative) pulses applied to the gate

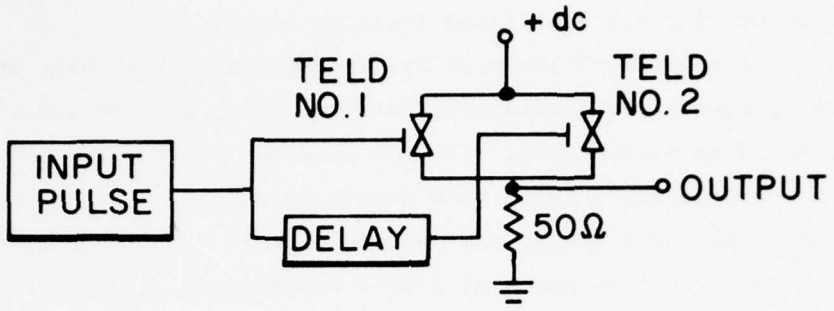


Figure 48. Summing circuit.

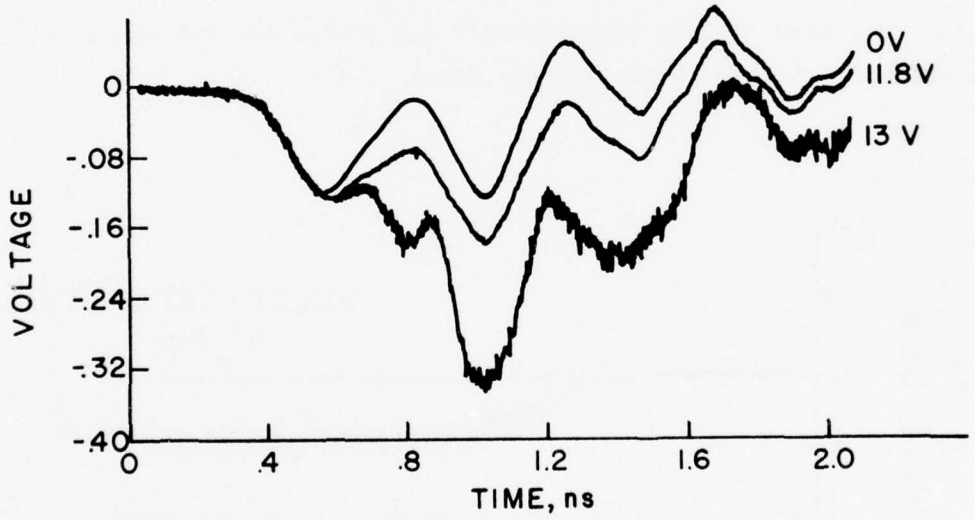


Figure 49. Output waveform of summing circuit.

with one delayed by 400 ps. The upper waveform, for 0-V bias, shows the feedthrough voltages which are due to the packaging capacitance of the devices. The two negative peaks are the differentiated lead edges of the pulses and the two positive peaks are the differentiated trailing edges.

The waveform in Fig. 49 produced by application of 13-V bias shows a large negative signal during the overlapping interval only, and the small feedthrough voltage can still be seen. About 1/3 V is produced in this test and this is sufficient for triggering a third TELD memory circuit.

The cathode of the TELDs in the summing circuit were connected to the gate of a TELD memory circuit by means of a 50-Ω transmission line to form the coincidence circuit shown in Fig. 47. The previous output was applied to the transmission line impedance rather than the 50-Ω resistor used previously. RF chokes were used for dc-bypassing in the transmission line. The anode bias of the third TELD was adjusted so that the output signal produced by a single input TELD (approximately 0.8 V) is not sufficient for triggering, while the signal produced by both TELDs (approximately 0.36 V) is sufficient for triggering. Each gate of the input TELDs requires a signal of 1.4 V. The final output signal for the third TELD is approximately 0.2 V when the two input pulses are time coincident. Figure 50 shows these data.

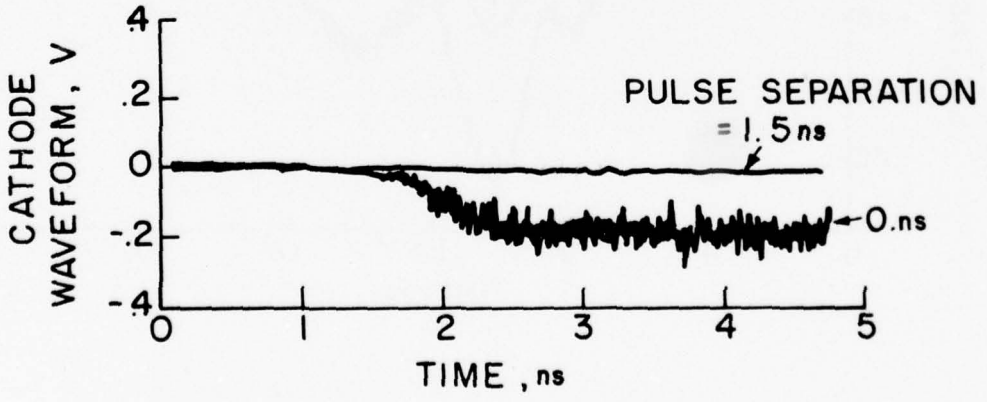


Figure 50. Output of three-TELD coincidence circuit.

The insertion delay time of the breadboard "AND" and "LATCH" circuit combinations was measured to be 1.5 ns plus the rise time of the output step. Approximately 0.7-ns delay time is directly attributable to transmission lines so that the output can certainly be made to occur with less than 1-ns insertion delay, as required in the TDOA system. In fact, a total insertion delay of less than 0.5 ns should be realizable using unpackaged devices and short transmission lines where required.

The amplitude of the output step in Fig. 50 is much less than desired for control of the clocks. The use of TELDs with larger current drop will enhance the output voltage significantly. Furthermore, if anode output is used instead of cathode output, about six times the output voltage is available. The difficulty is that the output impedance of the anode circuit is six times higher and if the physical separation of the coincidence circuit and clock requires a transmission line connection, transmission lines of this characteristic impedance are difficult to realize.

The coincidence circuit with resistive combining of signals is simpler in design. Figure 51 shows such a circuit. Here signal loss at the gate must be accepted in order to provide isolation between input lines. In the breadboard module, the input signals will be brought to the coincidence circuit via 50-Ω transmission lines. A mismatch (i.e., reflection coefficient) greater than 15% is undesirable. Likewise, greater than 15% input-to-input transmission is undesirable. A choice of R_1 = 40 Ω and R_2 = 20 Ω would produce 17% input (voltage) transmission and 6% input (voltage) reflection. However, only 31% of each input signal will be applied to the gate of the TELD.

The use of a split-gate TELD eliminates the input isolation problem. Each input goes to a separate section of the gate and the coupling between sections is small. A matching resistor for the input lines is still required.

A split-gate TELD was used to construct a dual input coincidence circuit. It is similar to the circuit of Fig. 51 except each input goes to a separate gate and R_2 = 200 Ω. The cathode (viewing) resistance is 50 Ω. The device used has transit-time frequency of 5 GHz and shows about 23% current drop on the curve tracer.

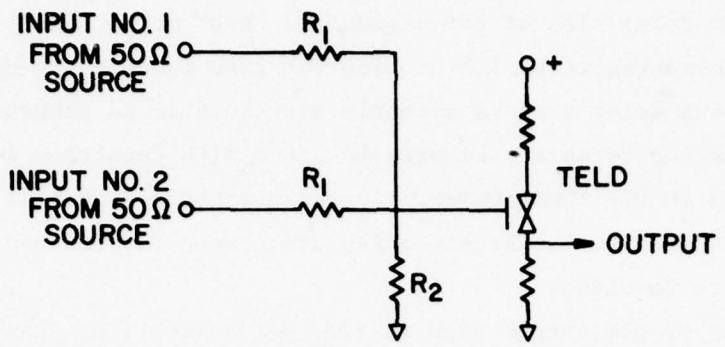


Figure 51. Single TELD coincidence circuit with resistive addition.

Tests were made to determine the minimum gate pulse height needed for triggering a domain at coincidence but with no triggering for time separation of gate pulses. Reliable operation was found for a minimum of 1.1 V on each gate line. The input pulse width (at half-height) was approximately 320 ps. As the delay between gate pulses was made to exceed about 225 ps, no triggering would occur. This is excellent performance for this circuit and indicates that if narrower input pulses were available, much smaller time resolution could be obtained.

Figure 52 shows the experimental data. The triggered state shows transit-time oscillation with period of approximately 200 ps. This is the data for the case of zero time delay between channels. The other data are for a delay of 225 ps. These data are similar to all data obtained for larger delay. No current drop is present for delay greater than 225 ps.

Approximately the same output signal as seen in Fig. 52 could be obtained by triggering a single gate with a larger input voltage. In a separate test it was found to take 1.1 V on each gate or 1.7 V on a single gate for the same output signal. Thus, it requires about 50% more signal to trigger one gate as compared with two equal input signals on the split gate.

The split-gate coincidence circuit could not be used in the breadboard module because the gate signal available in each channel of the module is about 0.5 V. This is insufficient for operation of the present split-gate devices.

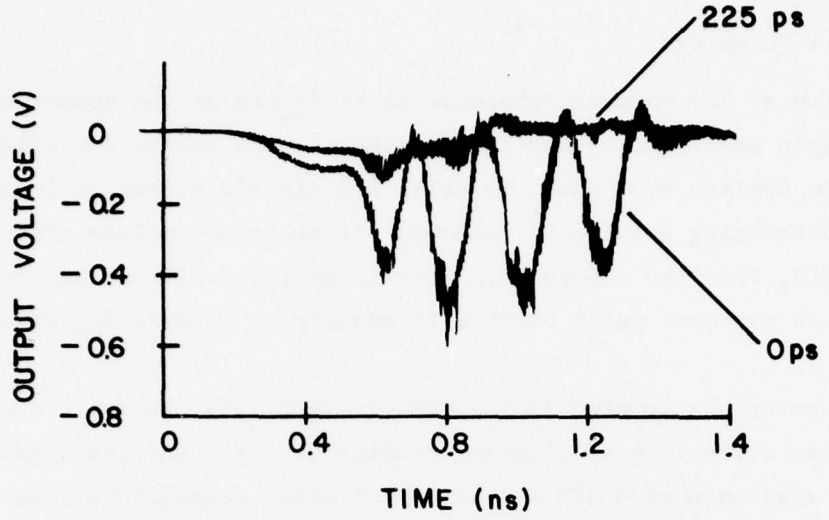


Figure 52. Output voltage waveforms as a function of time for the split-gate, TELD coincidence circuit with 24 mA of current. The input pulses are 1.2 V and have the time separation noted.

2. Breadboard Design

The amplitude of the pulses in both the clock and vernier channel pulse burst was found to be approximately 0.5 V. Since the performance of the single-gate TELD coincidence circuit is best for above 0.5-V input pulses, it was decided to directly sum the pulse trains and to apply this sum to the gate of the coincidence TELD. This permitted the threshold voltage to be set somewhat below 1.0 V. The resistors R_1 and R_2 (Fig. 51) were chosen to be 0 and 100 Ω, respectively. Although this design permitted the TELD to operate with best choice of input voltage, the signal transmission between clock and vernier channels was made very large. In order to eliminate any undesirable effects, a delay line was inserted in each channel before the connection to the coincidence circuit. About 2.5 ns is added to each line. The use of a split gate TELD in the coincidence circuit will eliminate the need for delay line. However, if some delay proves necessary, it must be matched with some delay added to the clock signal going to the vernier counter. This is because the output of the coincidence circuit must arrive less than 1 ns after the start of the clock signal at the vernier counter.

D. HIGH BIT RATE COUNTERS

1. The Counter Subsystem

The function of the Counter Subsystem is to determine the number of pulses in the pulse train generated by the clock pulsers. The counters available are ECL type and can operate at 1 GHz. By using the clock's output as input to the counter, the interfacing problem is reduced. If the clock pulses are about 0.5 ns at half-height, then the counter can operate properly without any interfacing circuits. A much narrower pulse width will require an interfacing square wave generator.

The most convenient counter is a 1-GHz divide-by-ten counter. The divide-by-ten output can connect to a following counter if the count goes past 10. All counts are available with BCD outputs which would normally be read after the counter is stopped. These outputs will not follow the inputs at 1-GHz toggle rate. There is estimated to be about 4-ns delay per decade for these counters. Thus, it could take about 8 ns to count to 100.

Input voltages of 0.25 to 0.5 V are required for proper counter operation. These values can be achieved with TELDs.

2. Experimental Evaluation

The performance of an RCA TC1113 divide-by-four counter was evaluated using pulse groups on the input. The width (at half-height) of the pulses was 3 ns and the spacing was 15 ns. Input pulse groups of 4, 8, and 12 produced output pulse groups of 1, 2, and 3, respectively. The shortest pulse group that could be produced was four pulses of 0.6-ns duration and 2-ns spacing. A single output pulse resulted, as shown in Fig. 53. The problems found were the lack of reset control and the lack of output information for pulse groups not a multiple of 4. A divide-by-two counter, presently under development by RCA would not have these difficulties.

The performance of a MECLIII, MC1696 divide-by-ten counter was evaluated using both pulse groups and cw rf signals on the input. The divide-by-ten output and the BCD outputs functioned properly for pulses of 3-ns width and 22-ns spacing. Figure 54 shows a photograph of the input and output pulses. CW operation to over 1200 MHz was achieved. The divide-by-ten counter is the simplest to utilize in the TDOA system.

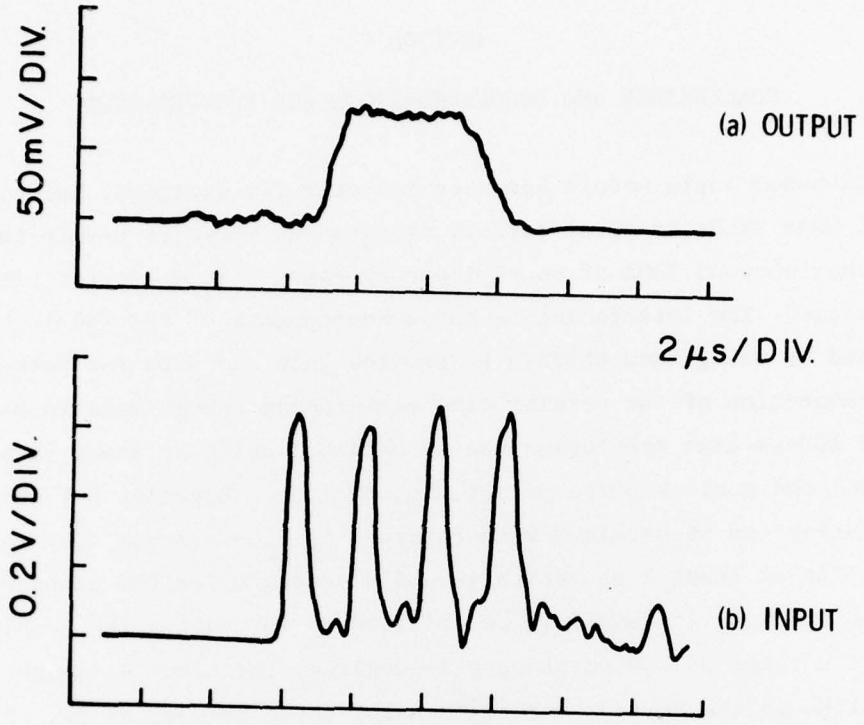


Figure 53. Input and output waveforms of the divide-by-four counters.

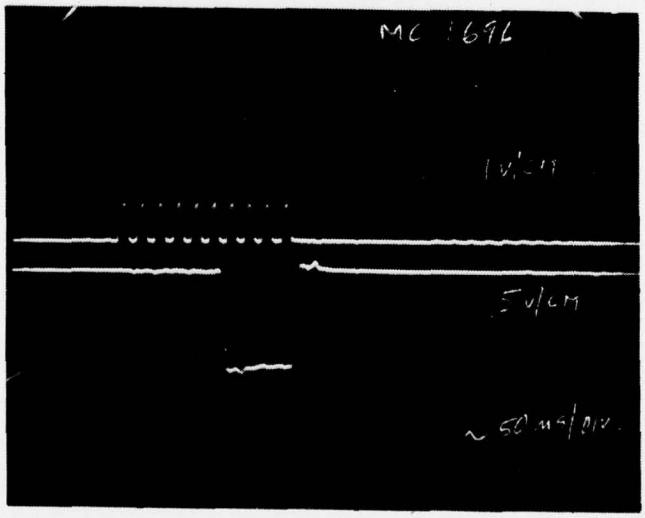


Figure 54. Input (upper trace) and output (time trace) of the divide-by-10 counter (scale is 50 ns/div).

SECTION V

CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER STUDY

A TELD-based logic module has been successfully designed, built, and tested. The use of GaAs TELDs in novel circuit designs was shown to permit the measurement of subnanosecond TDOA of an rf input by means of the vernier time measurement technique. The interfacing of the subcomponents of the module has been accomplished by using GaAs MESFETs to provide gain and SRDs for pulse sharpening.

The inspection of the vernier time measurement scheme made in Section II shows that 100-ps time resolution can be obtained using at least 11 pulses in each channel and a clock pulse period, T_C, of 1 ns. Equation (4) shows that the same resolution can be obtained with 8 pulses if $T_C = 0.7$ ns. The range of the measurement is at least 2 ns, which is quite adequate for the proposed TDOA system. An increase in range can be obtained by increasing the number of clock pulses. If a range of 100 ns or more is desired, the clock's design must be changed, although the vernier burst generator could be used as is. Since there are applications for larger range systems, the design of such clocks should be pursued in future studies.

The threshold gate design was shown to convert the input rf waveform to an output pulse, when the input exceeds a threshold. This gate utilizes a TELD for thresholding, a MESFET for gain, and SRDs for pulse forming. This threshold gate was used as the first stage in both the clock and vernier channels in the logic module. Further development of this design may be worthwhile since the ability to trigger on GHz-rate signals and provide a latched output may be useful for other applications.

Five different designs of pulse burst generators (or clocks) have been constructed and evaluated. The two-terminal TED clock produced 70-ps pulses but could not be triggered properly for operation in the logic module. The most promising design studied is the triggerable TELD subharmonic oscillator. Although it was not used in the breadboard module this circuit could be developed into a very compact clock with an unlimited number of pulses. This would be useful for TDOA application requiring much larger range. Further study should be made of this design.

The most dependable clock circuit presently is the transmission-line/FET design and this was used in the breadboard logic module. Some future effort to make this circuit more compact and to reduce the pulse broadening effects would be worthwhile. Although a four-pulse clock was used in the breadboard module, an eight-pulse design was demonstrated.

Three different designs of TELD coincidence-circuits were constructed and tested. Although both the three-TELD circuit and the split-gate TELD circuit worked well, a single TELD with resistive signal-combining was used in the breadboard module because of its simplicity and good triggering sensitivity. However, this circuit permitted the input signals to couple together. To eliminate any problems caused by this, additional signal delay was added to each input line. The use of the single, split-gate TELD in the coincidence circuit is more desirable since it eliminates signal coupling and the need for any signal delay lines.

Commercially available, divide-by-ten, ECL counters were tested and found to be suitable for use in the logic module. If the clock rate significantly exceeds 1 GHz, then a state-of-the-art counter is necessitated. The breadboard logic module does not contain counters and some interfacing problems must be resolved in future work. The major problem is to boost the output of the coincidence circuit to properly disable the counting function.

The experimental tests of the breadboard logic module have clearly demonstrated the resolution of $T_C - T_V \approx 0.4$ ns. The time accuracy depends upon the time-averaging scheme. The equipment calibration was shown sensitive to the adjustment of the threshold condition on the input TELD threshold gate. An arrangement whereby calibration is maintained under microprocessor control was described. This should be studied in the future.

Future efforts should be devoted to achieving 100-ps resolution in a compact TDOA logic module. The use of a clock design based upon the triggerable TELD subharmonic oscillator should enable a significant size reduction as well as a large increase in measurement range, which is desirable for other applications of the TDOA system. The next effort should also achieve complete interfacing with commercial counters and means for data averaging.

REFERENCES

1. D. Martin, "Measure Time Interval Precisely," Electronic Design, 24, 162-167 (November 1974).

2. R. G. Baron, "The Vernier Time Measuring Technique," Proc. IRE, 45, 21-30 (January 1957).

3. J. Vanderwall, H. W. Hattery, and Z. G. Sztankay, "Subnanosecond Rise Time Pulses from Injection Lasers," IEEE J. of Quantum Electron., QE-10, 570-572 (July 1974).

4. W. R. Curtice, *Microwave Frequency Memory Using GaAs Transferred-Electron Devices,* Interim Tech. Report, Office of Naval Research, Contract No. N00014-74-C-0371 (December 1974).

GLOSSARY

Chip Resistors - 0.1" x 0.1" pieces of alumina with resistive deposit, used as resistors in circuits.

Coincidence Circuit - a circuit producing an output only when two inputs are in time coincidence.

FET - a GaAs MESFET (field-effect transistor) chip.

Pulse Width (Half-Height) - the time duration between half-maximum values in a pulse.

SB-Gate - Schottky-barrier gate in a semiconductor device.

SRD Circuit - step recovery diode circuit.

TDOA - time difference of arrival.

TED - transferred-electron device, usually a two-terminal device.

TELD - transferred-electron logic device, usually a three-terminal device.

TELD Gate - a logic gate constructed with a TELD.

T_C - time period of the clock pulses.

T_R - time resolution, equal to $T_C - T_V$.

T_V - time period of the vernier pulse generator.

Vernier Channel - the late channel. A channel with same time delay over the minus (a clock) channel.

APPENDICES

APPENDIX A

LOGIC FOR DERIVATION OF EARLY AND LATE CHANNEL SIGNALS

A practical logic module will require logic for determining which antenna (or channel) receives the earliest signal. In addition, the channel signals must be properly routed. The early signal goes to the (main) clock circuit while the late signal goes to the vernier circuit.

The circuit for determining which channel is early can be made by using a TELD "inhibit" circuit, with memory. The inhibit circuit consists of two TELDs in series, with each gate connected to a different channel. The first TELD pulsed will turn on and not permit the second TELD to turn on when gate-pulsed. The voltage node between the TELDs will be high if the lower TELD is on and low if the upper TELD is on. Thus, a check of this voltage value tells which channel is early.

The routing of the signals to the clock and vernier circuits must be altered from that of the breadboard layout. Figure A-1 shows one possible circuit for derivation of proper early and late pulses for the clock and vernier circuits, respectively. Step inputs from the threshold memory gate are fed to a summing network which could be resistive (as shown) or a dual gate FET. The summed signal output will then have two steps of known voltage values. The earliest step is processed by the SRD pulse shaping circuit to produce the early pulse for the clock circuit. Since the series SRD chops off the pulse width, the second step is ignored. The Schottky-barrier diode is back-biased by the amount of the first voltage step. Thus, the second (or late) step passes into the lower SRD circuit and a late pulse is derived for the vernier circuit.

A laboratory test was made of the SRD circuit with a packaged Schottky-barrier blocking diode (type HP2810). Figure A-2 shows the experimental circuit and Fig. A-3 shows the test data. A two-step input pulse was used and bias was arranged to block the first step. Figure A-3 shows that the pulse output did properly occur at and follow the time position of the second step. However, an early pulse does occur due to capacitive feedthrough by the Schottky-barrier diode. This undesired first-step transmission is 14%, whereas the desired second-step transmission is 57%. Thus, there is about a factor of 4 (i.e., 57%/14%) discrimination in this experimental circuit. This factor can be

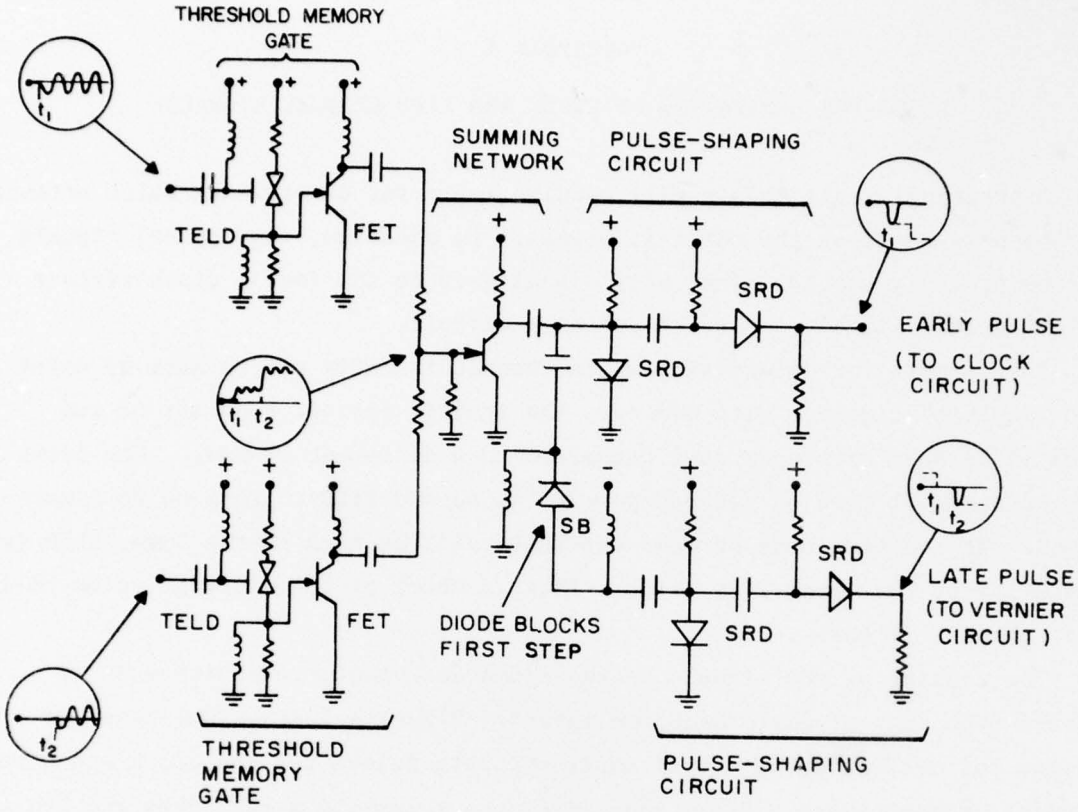


Figure A-1. Circuit suitable for separation of early and late channel signals.

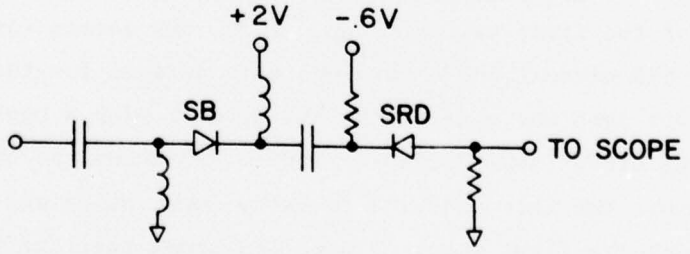


Figure A-2. Laboratory circuit for signal separation tests.

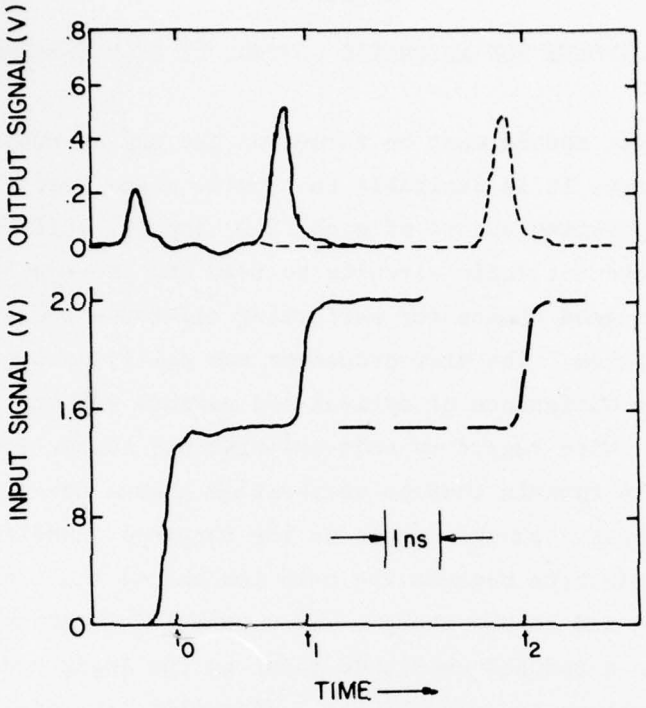


Figure A-3. Experimental data for the circuit of Fig. A-2.

improved by using a smaller area, unpackaged Schottky-barrier diode. Therefore, this test shows that the signal separation scheme is practical.

APPENDIX B

EQUIPMENT FOR AUTOMATIC CONTROL OF TELD THRESHOLD

Since the logic module must be turned on and may be subject to a range of ambient temperatures, it is desirable to provide means for: (1) automatic adjustment of the operating points of each TELD, and (2) self-calibration. Since there is also a need for logic circuits to read and process the output of the decade counters, a good choice for performing all these operations is a microprocessor-based system. The microprocessor can easily acquire the counter data, calculate the time difference of arrival and perform any statistical manipulation of the data. With regard to self-calibration, inspection of the operation of the logic module reveals that no calibration change can occur (in a calibrated module) unless a change occurs in the threshold condition of the input TELD gates. This is true because the path lengths of the clock and vernier channels are fixed and cannot change. If a path length change occurred in an SRD circuit due to a reduced amplitude input to the logic module, the same change would be present in each channel. (Actually, the limiters preceding the logic module should eliminate this possibility). However, if one input threshold TELD drifted so that it triggered on a different voltage, then its output will occur shifted in time. Therefore, the need for automatic calibration is essentially elminated if the threshold condition of each input TELD can be held constant. Obviously, it is also desirable to hold constant the operating point of the TELD in the coincidence circuit.

Figure B-1 shows a novel system for automatically controlling the operating points of each TELD. Under microprocessor (μP) control, a test signal is applied to the Schottky-barrier gate of the TELD, the output response is processed by the μP and the μP then provides the proper adjustments of the dc bias of the Schottky-barrier gate of the TELD. The test signal should be, for example, a 40-μs negative voltage ramp, occurring at a low duty rate, such as once each second. Normal operation of the logic module would not be interfered with for such a short test time. Using a microprocessor with a clock rate of about 1 MHz should provide 5 or more output response samples which can be fed to the microprocessor through direct memory access (DMA), if necessary. The software in the microprocessor will then determine the bias adjustment to be

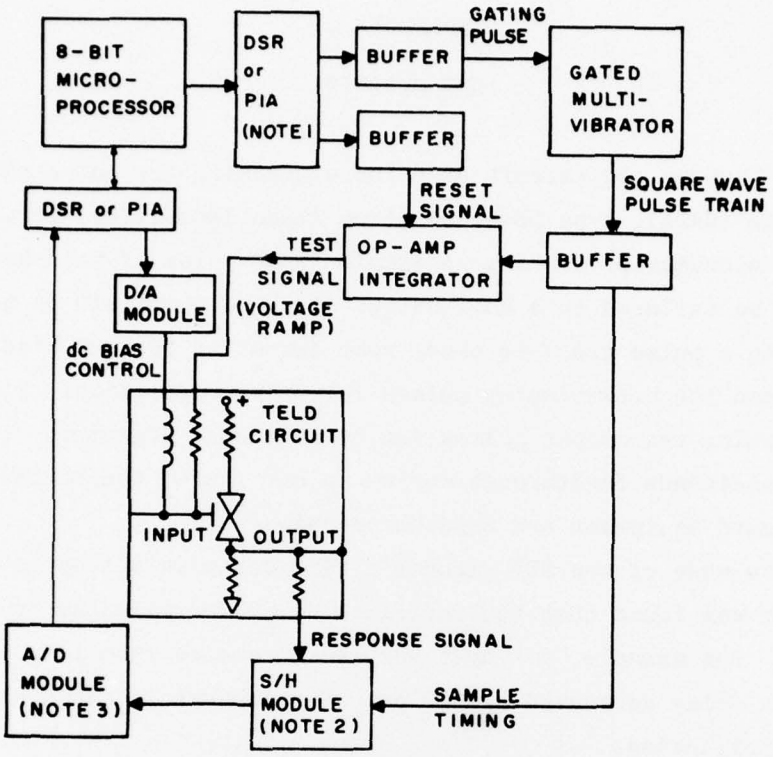


Figure B-1. Equipment layout for control of TELD threshold.
Notes: (1) input/output device select register of peripheral interface adapter;
(2) sample-and-hold module;
(3) analog-to-digital module

made on the TELD. The microprocessor will probably utilize the known (or previously tested) data on this TELD. The same microprocessor can control all three TELDs in this system.

A preliminary study was made of the components required for the equipment shown in Fig. B-1. The A/D and D/A modules used only eight bits and the A/D module requires about 1-MHz operation. The S/H module, multivibrator, and integrator must all work in the vicinity of 1 MHz. All these components are commercially available.

APPENDIX C

SRD CIRCUITS

Figure C-1 shows the circuit used for sharpening the pulse shape. Step recovery diodes (SRDs), type DBV6100A (from Alpha Industries, Inc., Woburn, MA) are used in a microstrip circuit. A single input pulse of half-height equal to 600 ps can be tailored to a half-height width of about 110 ps as shown in Fig. C-2. When a pulse train is used, some amount of forward-bias voltage is required between the back-biasing pulses for proper operation. With a proper input pulse train, the output pulses can be sharpened together. In order to reduce the capacitance feedthrough during an off state, the series SRDs used in the breadboard equipment are unpackaged chips.

Tests were made of the SRD circuit's time delay as a function of input amplitude. It was found that the insertion delay decreases as input voltage is increased. For example, as input voltage increased from 1 V to 2 V, the circuit's time delay decreased by 120 ps. Such behavior causes no problems in the TDOA application.

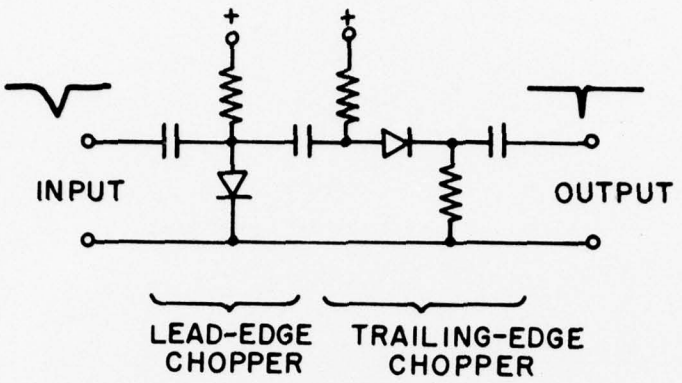


Figure C-1. SRD circuit used for pulse sharpening of subnanosecond pulser. Diodes are type DVB6100A from Alpha Industries, Inc.

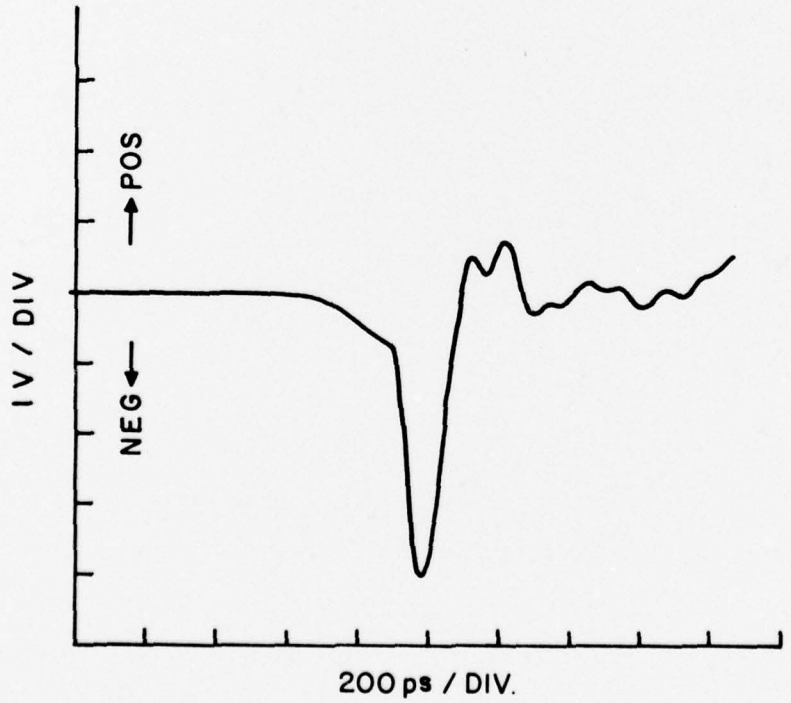


Figure C-2. Output of SRD circuit.